Lecture 2, ANIK

CMOS, Analog building blocks
Monday, January 23, 2012 in P26

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What did we do last time?

- Introduction to the course
  - Labs, quizzes, exam, etc.
- The transistor
  - Operating regions (cut-off, linear, saturation)
  - Functionality (output current as a function of the witdth and lenght)
- First amplifier and parameters

What will we do today?

Small-signal schematics

- Linearization

Further work on the analog building blocks

- Common-source, common-drain, common-gate, etc.

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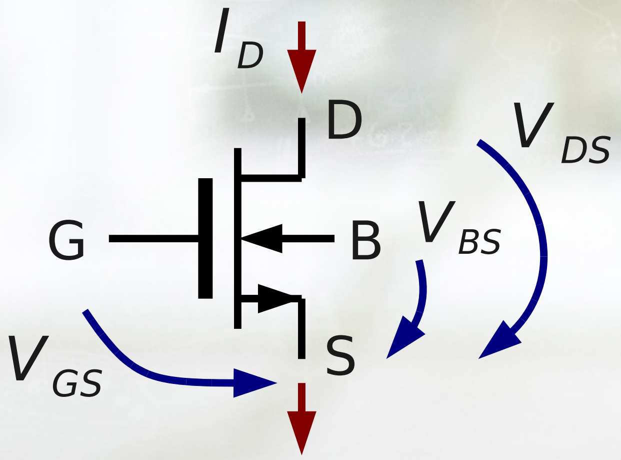
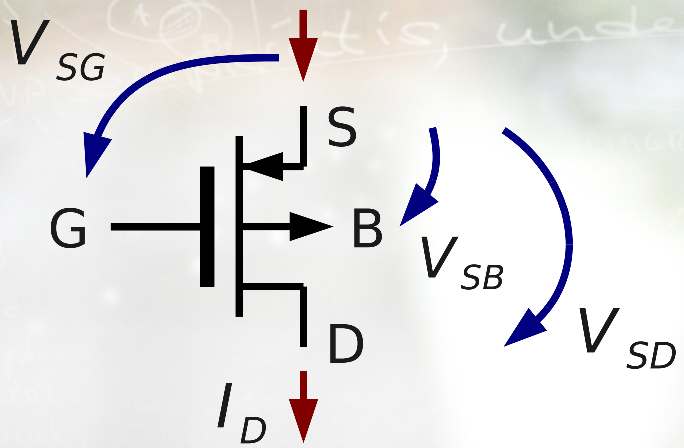
The transistor revisited 1



(a) NMOS



(b) PMOS

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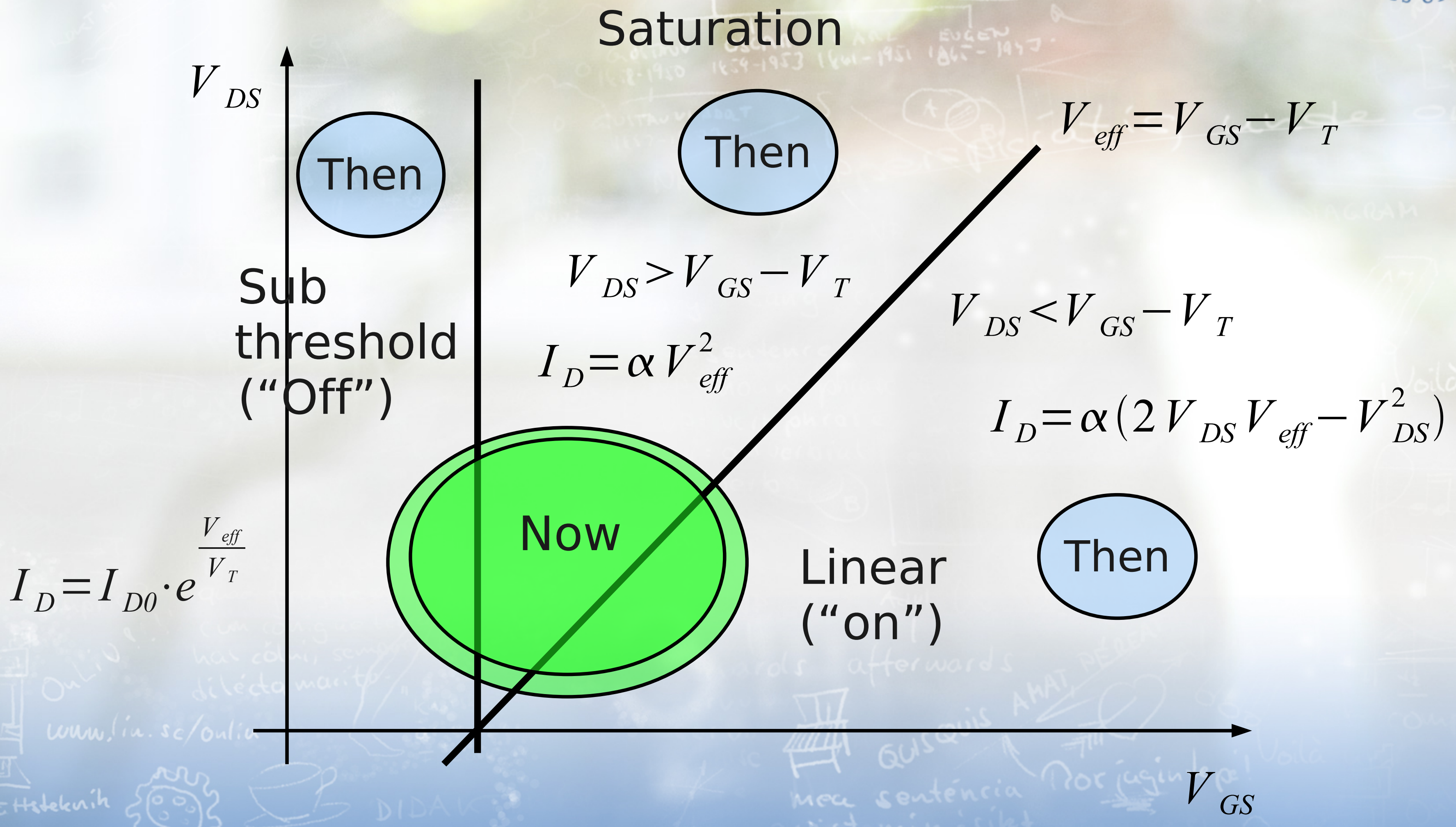
The transistor revisited 2



Saturation

V_{DS}

Then

Then

$V_{eff} = V_{GS} - V_T$

Sub threshold ("Off")

$V_{DS} > V_{GS} - V_T$

$I_D = \alpha V_{eff}^2$

$V_{DS} < V_{GS} - V_T$

$I_D = \alpha (2 V_{DS} V_{eff} - V_{DS}^2)$

$I_D = I_{D0} \cdot e^{\frac{V_{eff}}{V_T}}$

Now

Linear ("on")

Then

V_{GS}

The first amplifier revisited

A common-source amplifier

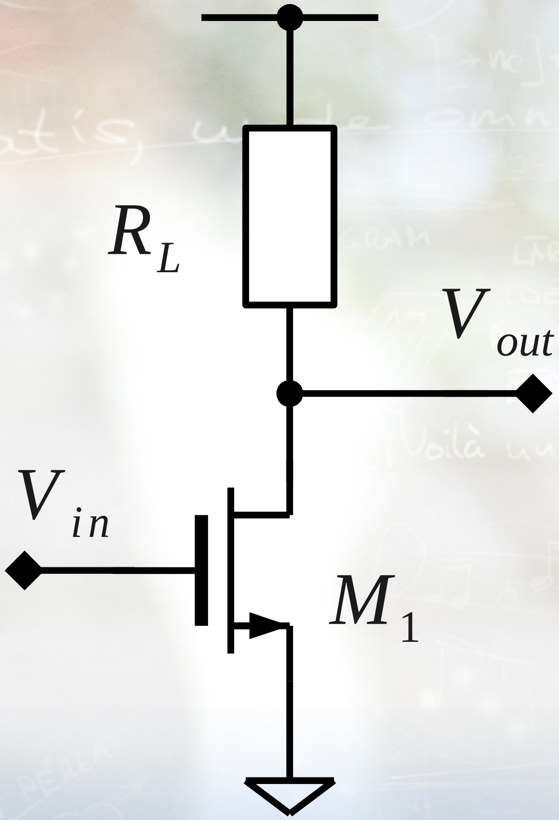
$$v_{out} = V_{DD} - R_L \cdot I_D$$

Saturation region

$$v_{out} = V_{DD} - R_L \cdot \alpha \cdot v_{eff}^2$$

Linear region

$$v_{out} = V_{DD} - R_L \cdot \alpha \cdot \left(2 v_{out} v_{eff} - v_{out}^2 \right)$$



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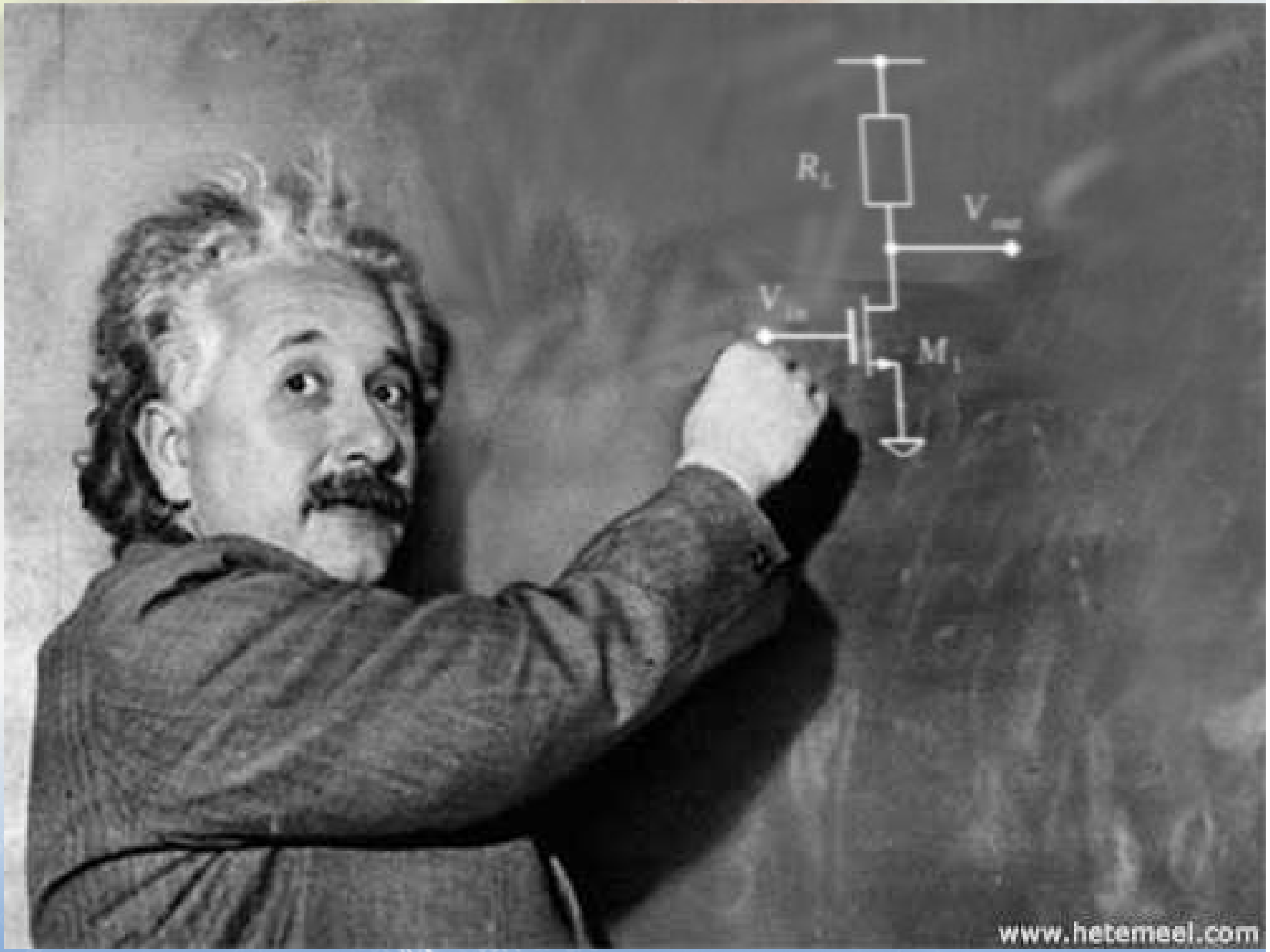
The first amplifier revisited

Large-signal transfer characteristics

Position of DC point

Other design requirements



Small-signal schematics

Linearization around a DC point

- Small variations around the DC point are assumed
- We will sum (superposition) the contributions from all different sources to the output
- (Linearization implies no distortion)

Notice that there might be a trade-off between swing and max gain

- The choice of DC point is non-trivial...

Linearization example

Original

$$I_D = \frac{\mu C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{gs} - V_T)^2 \cdot \left(1 + \frac{V_{ds}}{V_\theta}\right)$$

Apply partial derivation, i.e., linearize

$$\Delta I_D = \frac{d I_D}{d \mu} \cdot \Delta \mu + \frac{d I_D}{d C_{ox}} \cdot \Delta C_{ox} + \frac{d I_D}{d W} \cdot \Delta W + \frac{d I_D}{d L} \cdot \Delta L + \\ + \frac{d I_D}{d V_{GS}} \cdot \Delta V_{GS} + \frac{d I_D}{d V_T} \cdot \Delta V_T + \frac{d I_D}{d V_{DS}} \cdot \Delta V_{DS} + \frac{d I_D}{d V_\theta} \cdot \Delta V_\theta$$

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Linearization example, cont'd

We assume the physical parameters to be constant

$$\Delta I_D = \frac{d I_D}{d V_{GS}} \cdot \Delta V_{GS} + \frac{d I_D}{d V_{DS}} \cdot \Delta V_{DS} + \frac{d I_D}{d V_T} \cdot \Delta V_T$$

Apply the chain rule

$$\frac{d I_D}{d V_T} \cdot \Delta V_T = \frac{d I_D}{d V_T} \cdot \frac{d V_T}{d V_{BS}} \cdot \Delta V_{BS}$$

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Linearization example, cont'd

Introduce some nomenclature

$$\Delta I_D = \underbrace{\frac{dI_D}{dV_{GS}}}_{g_m} \cdot \Delta V_{GS} + \underbrace{\frac{dI_D}{dV_{DS}}}_{g_{ds}} \cdot \Delta V_{DS} + \underbrace{\frac{dI_D}{dV_T} \cdot \frac{dV_T}{dV_{BS}}}_{g_{mbs}} \cdot \Delta V_{BS}$$

and skip the deltas

$$i_d = g_m \cdot v_{gs} + g_{ds} \cdot v_{ds} + g_{mbs} \cdot v_{bs}$$

Which gives us a transistor "consisting" of three current sources

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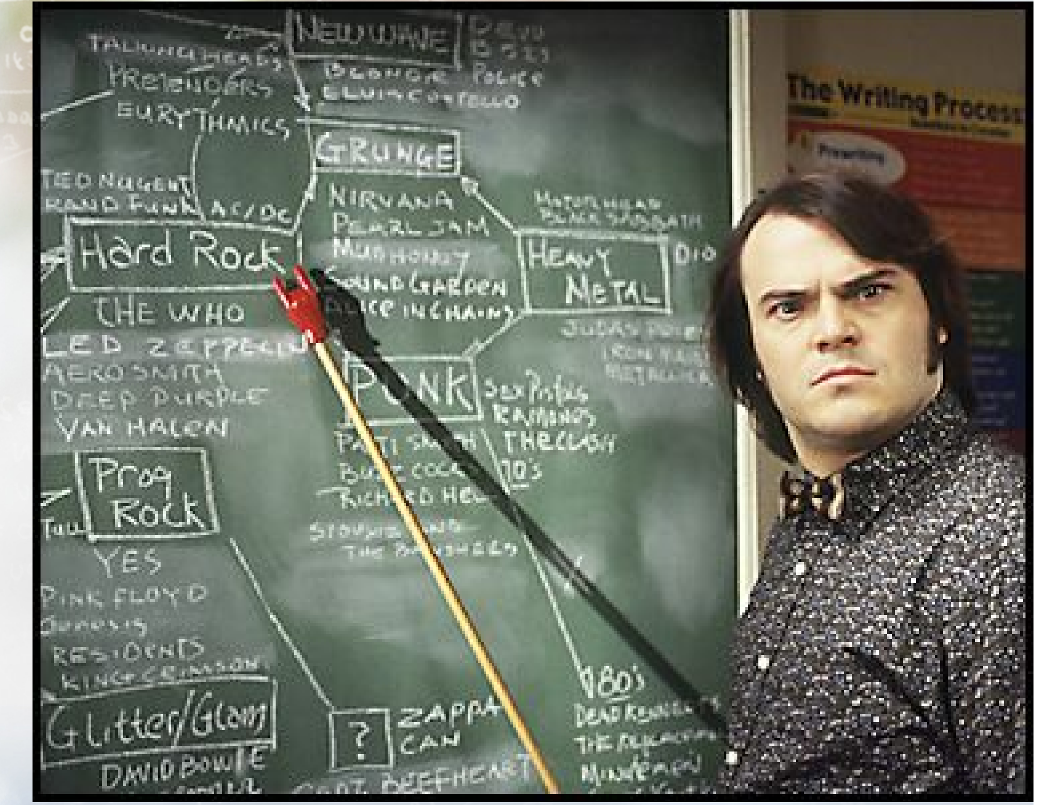
The small signal model and its impact

Illustration of the small signal model

Some calculations

(More practice in the lessons)



Transistors compiled

Expression	Cut-off	Linear	Saturation
g_m	$\frac{\kappa I_D}{kT/q}$	$2\alpha v_{ds}$	$\frac{2I_D}{v_{eff}}$ $2\sqrt{\alpha I_D}$
g_{mbs}	$g_m \cdot \frac{1-\kappa}{\kappa}$	$g_m \cdot \frac{\gamma}{2\sqrt{V_{SB}+2\phi_F}}$	$g_m \cdot \frac{\gamma}{2\sqrt{V_{SB}+2\phi_F}}$
g_{ds}	λI_D	$2\alpha\left(v_{eff}-v_{ds}\right)$	λI_D

How large are these values?

Transistor gain vs region

Expression	Cut-off	Linear	Saturation
$A=\frac{g_m}{g_{ds}}$	$\frac{\kappa \cdot q}{\lambda \cdot k T}$	$\frac{v_{ds}}{v_{eff}-v_{ds}}$	$\frac{2}{\lambda \cdot v_{eff}}$ $\frac{2\sqrt{\alpha}}{\lambda\sqrt{I_D}}$

? What can you spot (where is the gain highest) $\kappa \approx 0.75$ and $k T / q \approx 26$ mV.

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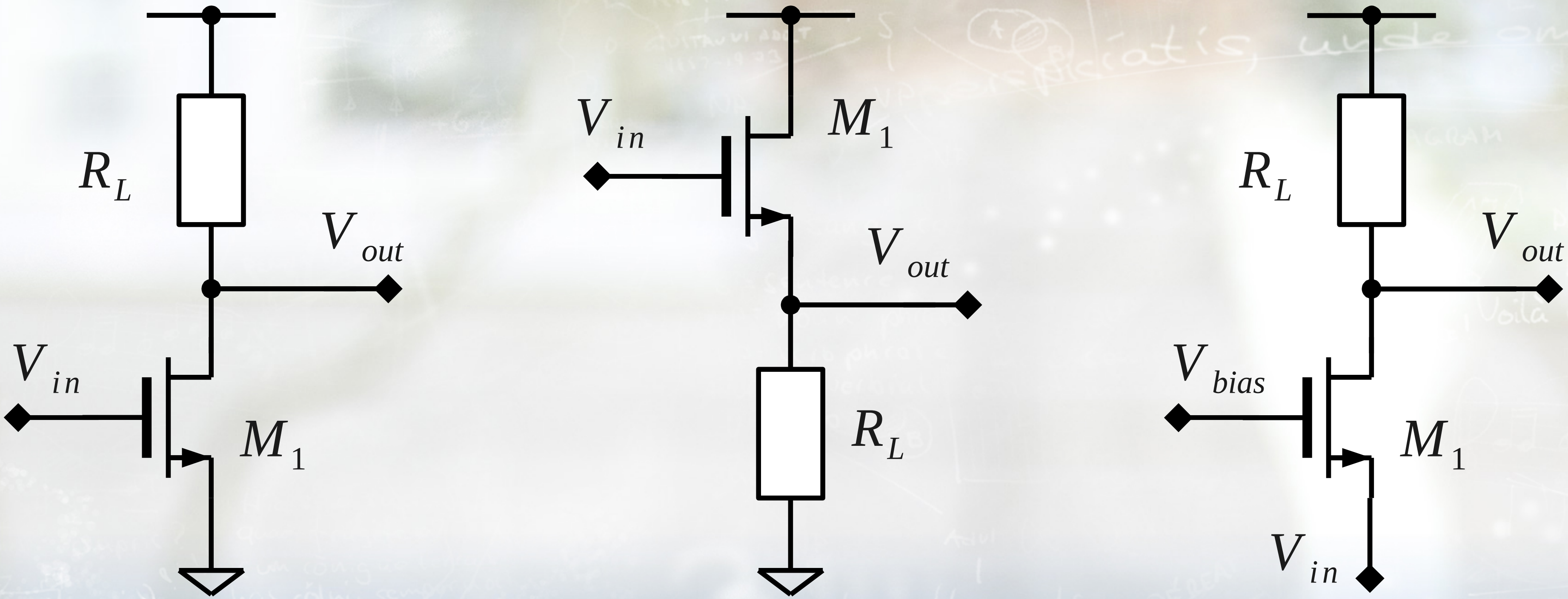
The three amplifier stages

With passive load



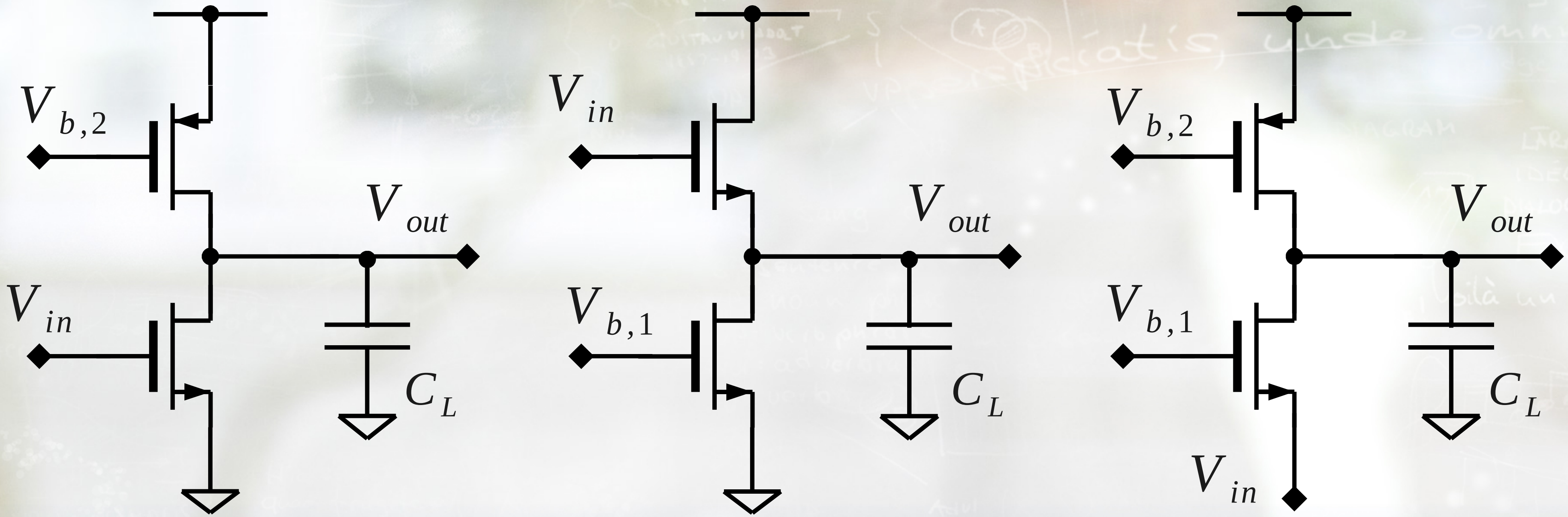
(a) NMOS CS

(b) NMOS CD

(c) NMOS CG

The three amplifier stages

With active load



Why active load?

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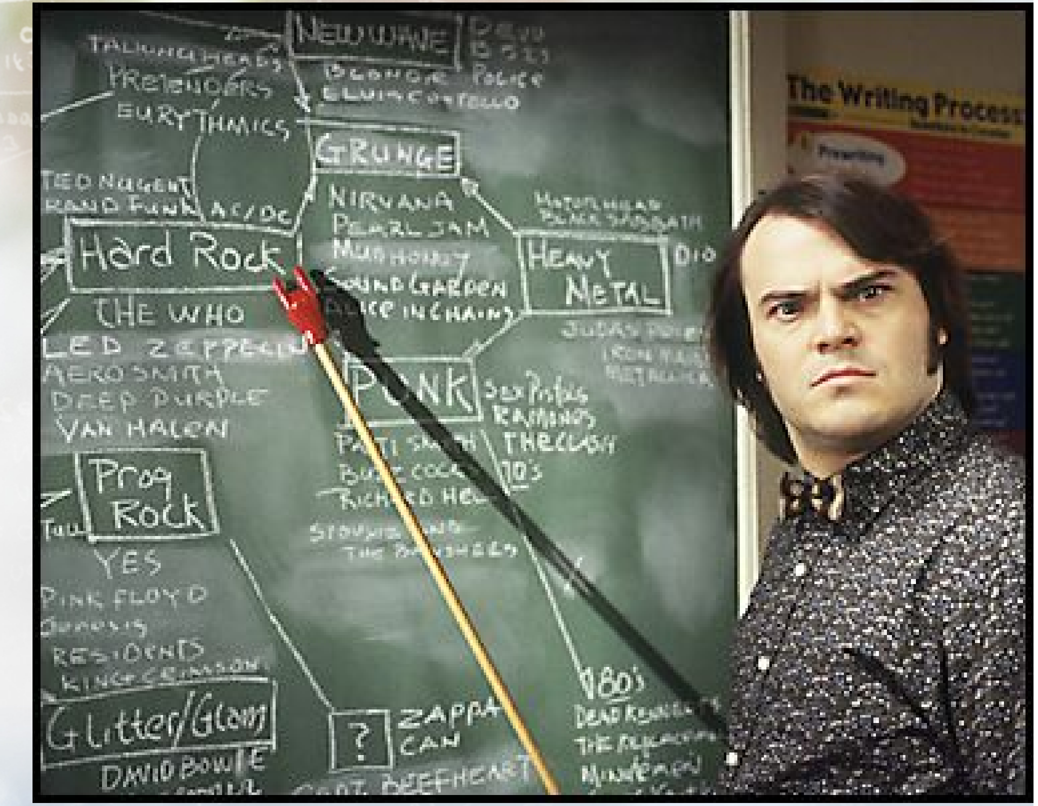
The small signal exercises

Using the small signal approach to

derive the gain



Amplifier stages, compiled 1

	Expression	**CS**	**CD**	**CG**
DC gain,	$A_0 \approx \frac{g_m}{g_{out}}$	$\approx \frac{g_m}{g_P + g_N}$	$\approx \frac{g_m}{g_m + g_P + g_N} \approx 1$	$\approx \frac{g_m}{g_P + g_N}$
Output impedance,	$\approx g_{out}$	$\approx g_P + g_N$	$\approx g_m$	$\approx g_P + g_N$
Input impedance,	$\approx g_{in}$	∞	∞	$\approx g_m$
Bandwidth,	$p_1 \approx \frac{g_{out}}{C_L}$	$\approx \frac{g_P + g_N}{C_L}$	$\approx \frac{g_m}{C_L}$	$\approx \frac{g_P + g_N}{C_L}$
Unity gain,	$\approx A_0 \cdot p_1$	$\approx \frac{g_m}{C_L}$	N/A (why?)	$\approx \frac{g_m}{C_L}$

Amplifier stages, compiled 2

Expression		CS	CD	CG*)
DC gain,	$A_0 \approx g_m / g_{out}$	$\approx 1/\lambda \cdot v_{eff}$	≈ 1	$\approx 1/\lambda \cdot v_{eff}$
Output impedance,	$\approx g_{out}$	$\approx \lambda I_D$	$\approx 2 I_D / v_{eff}$	$\approx \lambda I_D$
Input impedance,	$\approx g_{in}$	∞	∞	$\approx 2 I_D / v_{eff}$
Bandwidth,	$p_1 \approx g_{out} / C_L$	$\approx \lambda I_D / C_L$	$\approx 2 I_D / C_L \cdot v_{eff}$	$\approx \lambda I_D / C_L \cdot v_{eff}$
Unity gain,	$\approx A_0 \cdot p_1$	$\approx I_D / C_L \cdot v_{eff}$	N/A (why?)	$\approx I_D / C_L \cdot v_{eff}$

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Amplifier stages, compiled 3

Amplifier stage	When and what to use?
Common-source	High-gain amplifier with high output impedance and high input impedance. Drive capacitive loads, typically in feedback.
Common-gate	High-gain amplifier with high output impedance and "low" input impedance. Drive capacitive loads, typically in feedback.
Common-drain	Low-gain amplifier with "low" output impedance and high input impedance. Drive resistive loads, can be in open-loop.

What did we do today?

"Simple" amplifier stages

A single transistor can be troublesome enough ...

Small-signal schematics practice

Practice, practice, practice

How do we increase gain?

What are our handles?

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What will we do next time?

Swing

- How many transistors can we stack?

Improving the gain

- We need high gain - how do we do it?

Current mirrors

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