Linköping University

Reinventing research and education

Analog and discrete-time integrated circuits (ATIK)

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LiU EXPANDING REALITY

Lecture 1, ATIK

Introduction, CMOS

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Analog and

discrete-time integrated circuits

Abbreviated as ATIK (from Swedish)

What is analog?

What is discrete-time?

What is integrated circuits?

Organizers

J Jacob Wikner (Lectures, Lesson, Labs, Miniproject)

Ph.D. Linköping University, 2001
Ericsson, Infineon, Sicon, AnaCatum, Cognicatus, IVP, LiU

Prakash Harikumar (Lessons and Labs)

Ph.D. student
B.Sc., Thiruvananthapuram, Kerala, India, M.Sc., LiU
Cognizant Technology Solutions, Indian Space Research Organization

Web resources

WWW: http://www.es.isy.liu.se/courses/ATIK

WP: http://mixedsignal.wordpress.com

FB: http://www.facebook.com/mixedsignal

Twitter: @jjwikner

Studiehandboken 1

Aim:

The purpose of the course is that the attendee should get:

- fundamental knowledge wrt. analysis and design of analog and discrete-time systems integrated ni CMOS technology for system-on-chips (SOCs)
- an understanding for the purpose and need of advanced computer-aided deisgn tools (CAD), i.e., different analysis and synthesis methodologies using computers.
- an ability to use simulation tools for circuit design

Studiehandboken 2

Course contents:

- Integrated circuit components, such as PMOS and NMOS transistors, capacitors, switches, current sources
- Analysis with respect to feedback and stability.
- Integrated active filters.
- Integrated switched-capacitor filters: charge-redistribution, error sources, switches, transfer functions.
- Performance measures: Noise. Spectral density. Distortion.
- Integrated data converters: Integrated analog-to-digital and digital-to-analog converters.

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Studiehandboken 3

After the course is completeted, the students should be able to:

- describe the relationships between different parameters and performance measures for different types of integrated circuits and components.
- understand the influence due to limitations in performance of subcomponents on integrated filters, A/D and D/A converters
- specify OPs and OTAs to be used in larger systems
- perform charge analyses on SC circuits and understand the influence of non-ideal components on the transfer characteristics
- design integrated continuous-time filters given building blocks such as OPs, OTAs, switches, and more
- design integrated switched-capacitor filters
- describe the architecture and functionality of the most common types of A/D and D/A converters suitable for CMOS
- perform noise and distortion analysis on CMOS circuits and understand the impact on for example data converters

Studiehandboken 4

Course literature:

Johns and Martin: Analog Integrated Circuit Design, John Wiley & Sons, 1997 (main course book)
Gray, Hurst, Lewis, and Meyer: Analysis and Design of Analog Integrated Circuits
Allen and Holberg: CMOS Analog Circuit Design
Razavi: Design of Analog CMOS Integrated Circuits
Via the web distributed material.

Examination:

Written examination	4 ECTS
Computer simulations	2 ECTS

Computer simulations, PRA1 The student will together with other students in smaller groups hand in a compilation of their own work concerning circuit simulation exercsies. Note that the group exercises constists of a combined suite of laboratories. The report is the concluding, examination document. The schedule laboratories are resource hours and the students have to plan their own time.

Written exam (TENA) During the lectures five quizzes will be handed out. The answers will be returned during the same lecture. Out of five quizzes one can maximally obtain three points. These points can be accounted for in the written exam. The written exams contains of five exercises totalling 25 points. With correct quizzes, the student can obtain a total of 28 points. The grading is: 10p: 3, 15p: 4, 20p: 5.

Course background

Course has been around since the 1980's

- Constantly evolving (you are the guinea pigs)
- Material is updated (things have changed since 1980s)

New for this year

- Updated lessons material
- Clarified labs (?)
- Well-established quizzes in studiehandboken

Feedback from last year

Students found ...

the ratio between slides and board to be too biased towards slides

projects/labs to be OK

too many course books to choose from

too much material in our on-line folders

too difficult written examination

In overall positive grades (> 3.5)

Analog and discrete-time integrated circuits

What is analog (bar voltage/current)?

There are a lot of trade-offs

Design targets not as "orthogonal" as in digital design.

There are no good tools to support these trade-offs

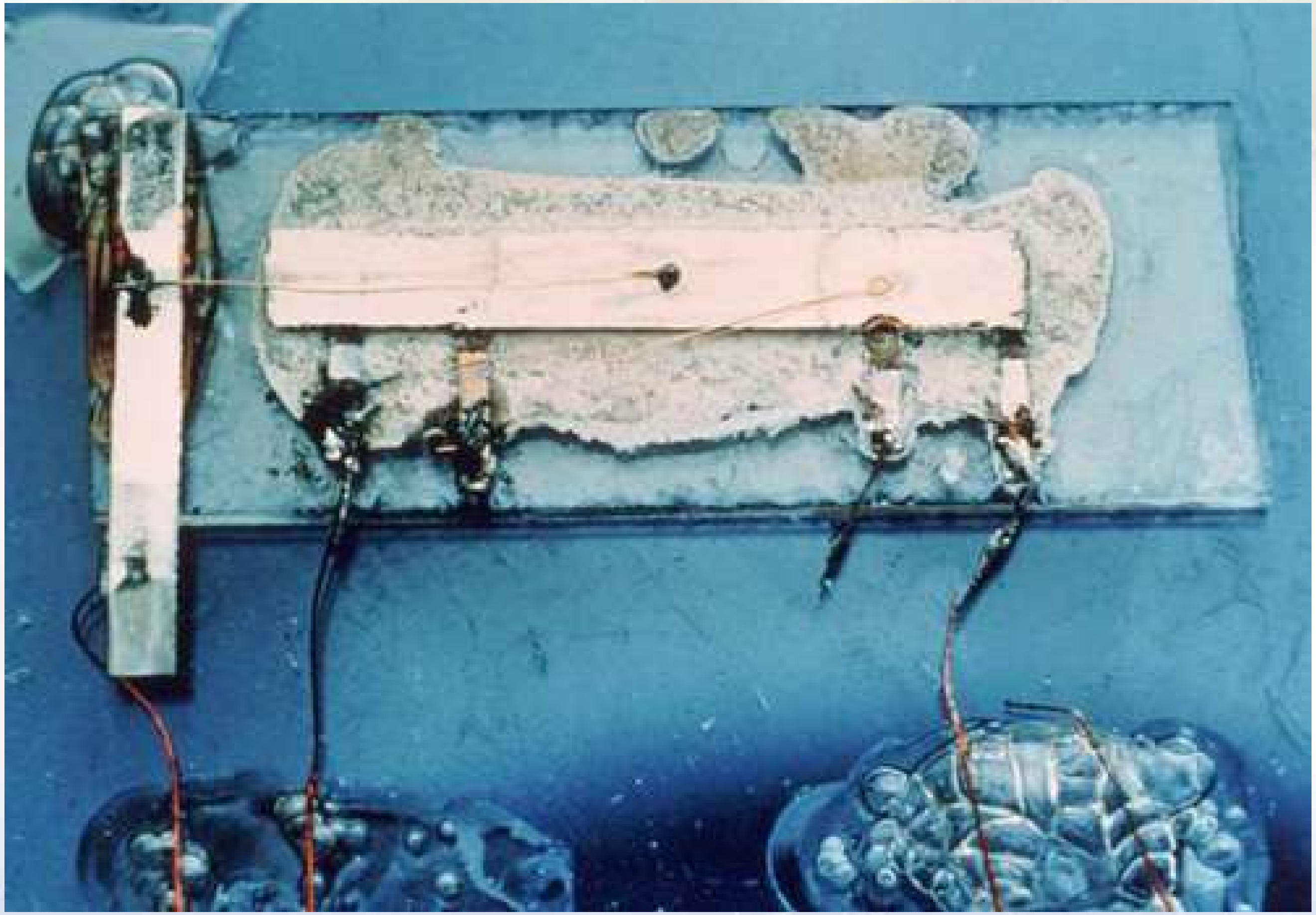
There is no automated synthesis (c.f., the systemC/RTL-to-FPGA flow)

There is no automated porting between new processes and geometries

A lot of guru knowledge required

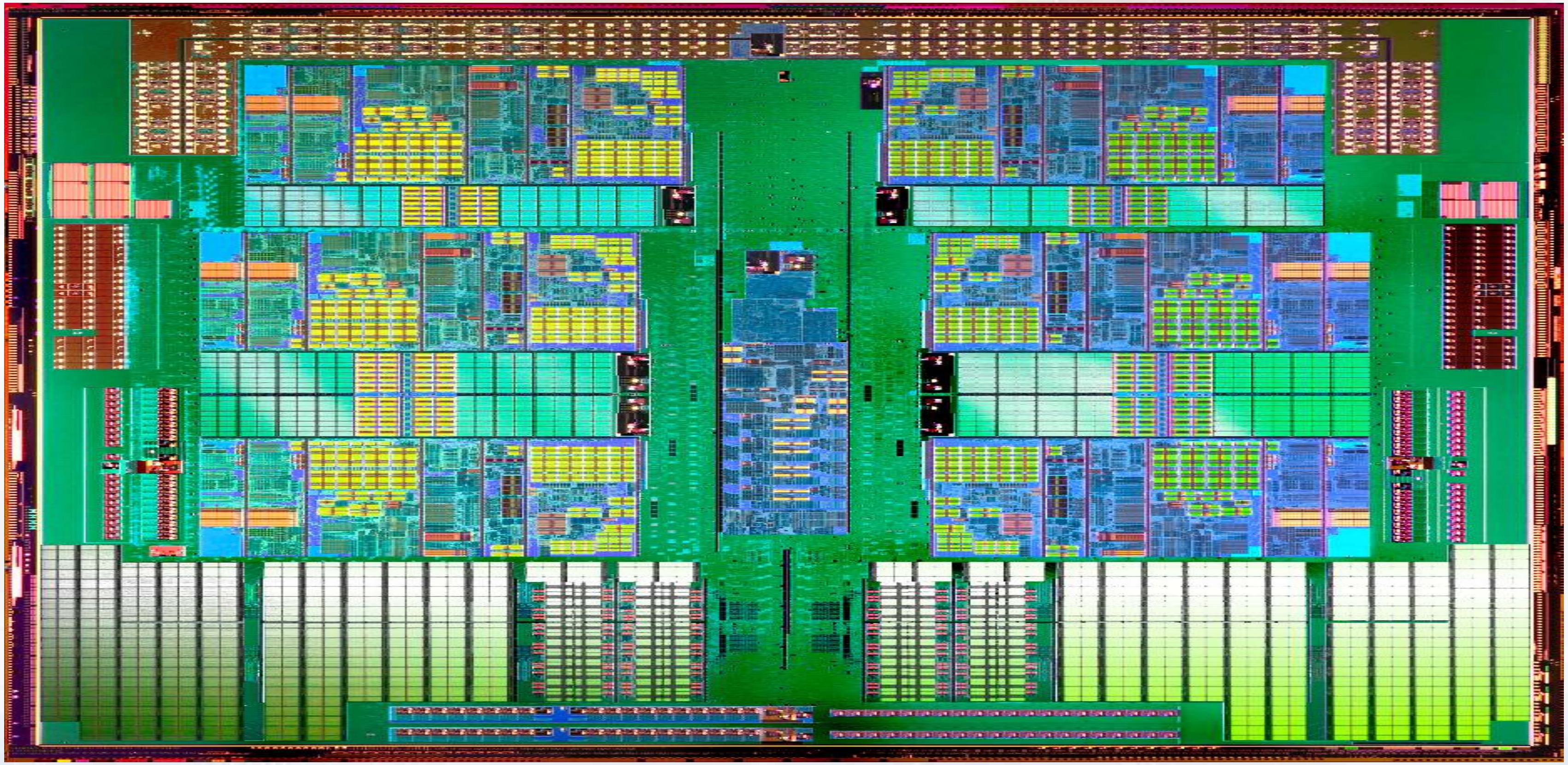
Analog and discrete-time integrated circuits @1947

Analog and discrete-time integrated circuits @1959



Courtesy of Texas Instruments

Analog and discrete-time **integrated circuits @2010**



Courtesy of Advanced Micro Devices, Inc. (AMD) (Stretched picture)

"Everything" will integrate into one single chip

- Mixed-signal integration
- RF integration
- Digital integration
- Memory integration
- Communication integration
- more and more

A brief history of time

Compare with Moore's law

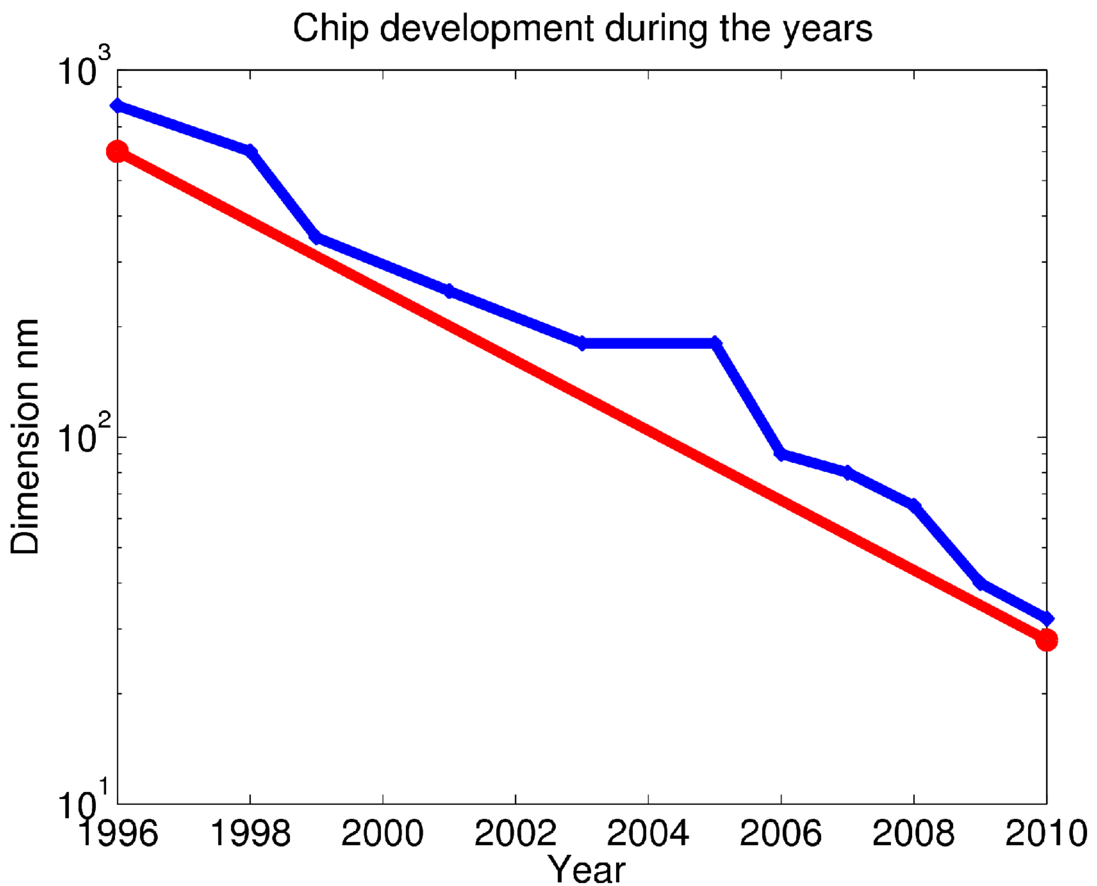
Every blah-blah month, the complexity doubles

Does analog scale?

With lower geometries, does analog become better - or worse?

What's the main limitation to development today?

Cost? Physics? Law-of-nature?



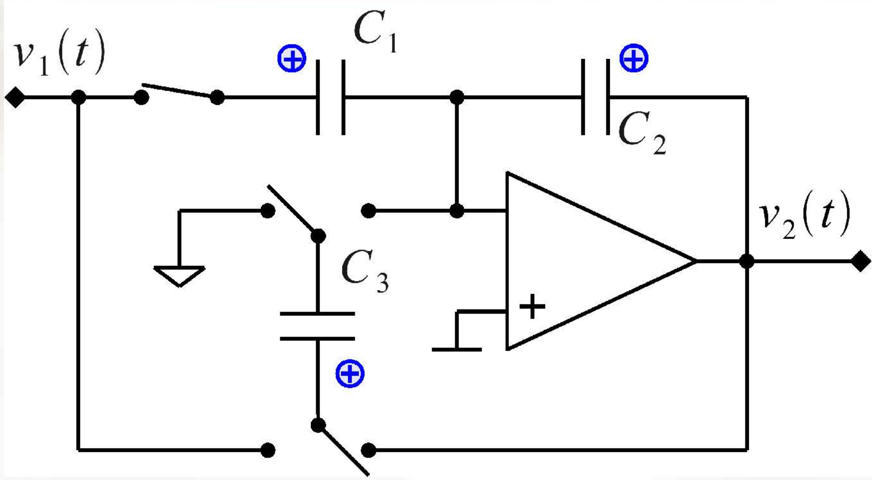
A brief history of time ...

Sampled systems

where the value can be continuous

updated at discrete time points

$$V(nT) = V((n-1)T) \cdot \frac{C_1}{C_2} + R_L \cdot I(nT)$$



Examples

Data converters (ADCs and DACs)

Switched-capacitor circuits and filter

Switched-current circuits

Books

Analog Integrated Circuit Design, Johns and Martin

Analysis and design of Analog Integrated Circuits, Gray, Hurst, Lewis, Meyer

CMOS Analog Circuit Design, Allen and Holberg

Design of Analog CMOS Integrated Circuits, Razavi

Analog Design Essentials, Sansen

Design of Analog Filters, Schaumann and van Valkenburg

Exam

Open-book exam

!!!

Any material can be brought to the exam

No calculators

Five exercises á five points

Be strategic

Pick your exercises

(... and why not take the exam in June instead? Learn from the Chip design ...)

Quizzes

Five random questions distributed

- One point on each
- Maximum three points that can be accounted for in the exam
- Valid for three exam occasions (March, June, August)
- You will get instant feedback

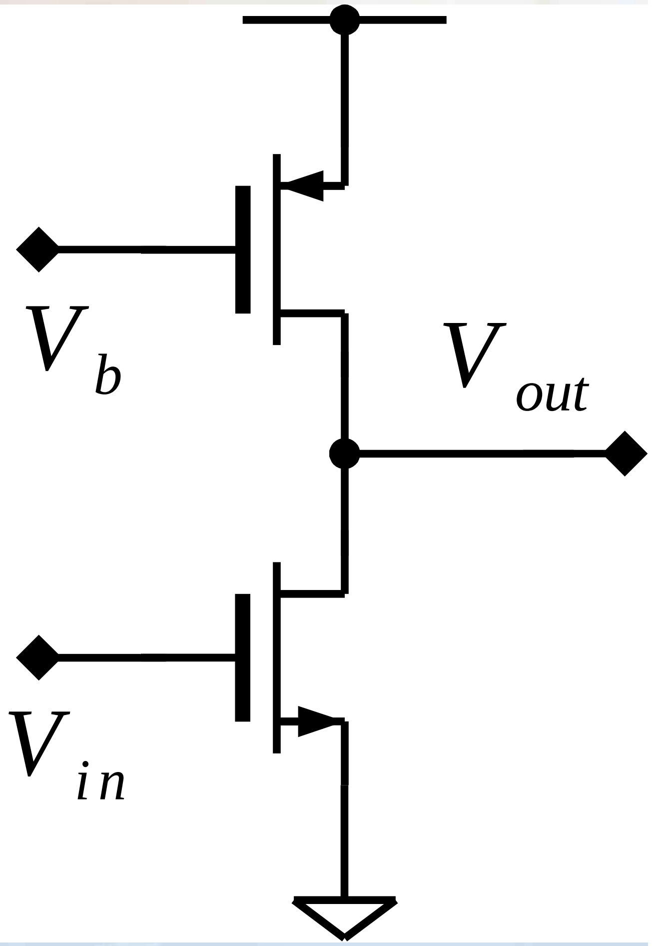
Quiz example

In a common-source amplifier, to minimize the output-referred noise, how should you design the gm of the active load?

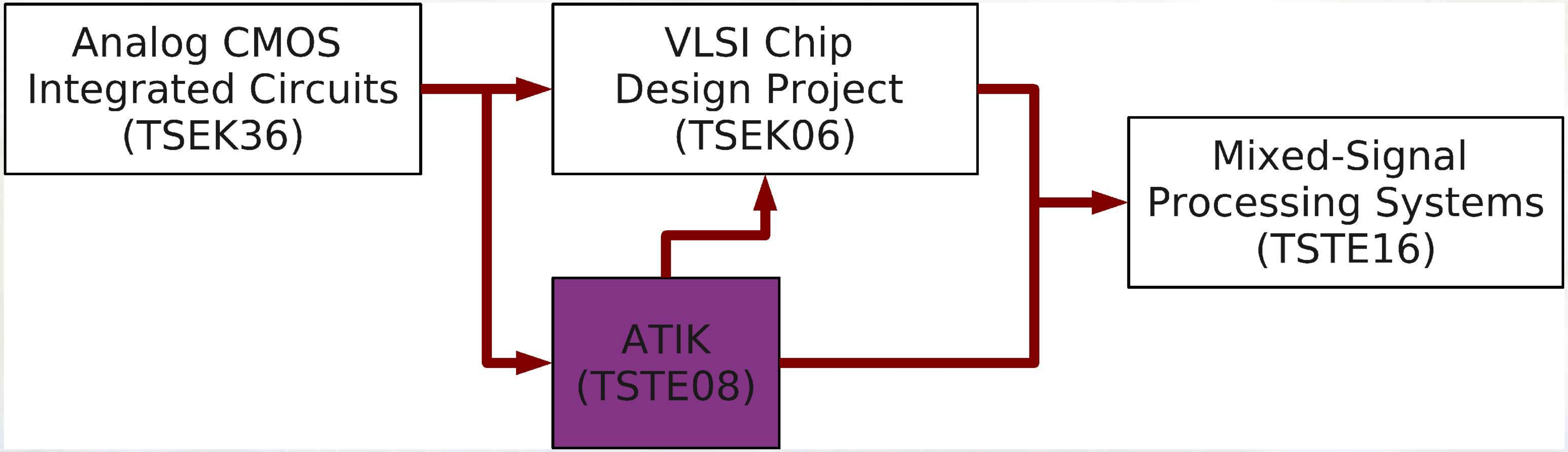
1) To be as high as possible

2) To be as low as possible

3) active load does not add any noise



Where does the course fit in?



Laboratory (miniproject)

Scheduled lab hours are resource hours

Three individual labs to be compiled into one lab report

(Max) Three students in each group. One is too few.

Why the miniproject?

The "miniproject" forms the lab report.

Deadline, last Thursday of May (by taking the VLSI course)

Course outline, compiled

Ten lessons follow ten lectures

more or less ...

Three laboratory

are recommended for ATIK

One miniproject

wrap up the labs in a report

Exam

Four-hours exam, bring (almost) everything (if you like)

Five quizzes

Randomly distributed, can give you three points.

Course outline - Lectures 1

#	TSTE08 ATIK
1	Introduction. Course overview, etc. Analog building blocks 1
2	Analog building blocks 2
3	Amplifiers 1 OP, OTA, Stability
4	Amplifiers 2 Noise
5	Switched capacitor 1 Basics, Accumulators

Course outline - Lectures 2

#	TSTE08 ATIK
6	Switched capacitor 2 S/H, Nonideal effects Continuous-time filters 1
7	Continuous-time filters 2 Discrete-time filters
8	Data converters 1 ADC and DAC basics
9	Data converters 2 Interpolating converters Sigma-delta converters
10	Data converters Case study (optional) Wrap-up

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"Conclusions": Why analog design?

(Except for the fact that an analog designer gets much more paid?)

Interface to the real world is analog (RF mod., sensors, etc.)

Today, the trend is towards SOC: integration of several different complex and advanced components on one piece of silicon

Always: go to digital as soon as possible

Then the data converters are your interfaces - and who designs them?

Where could this lead?

Linköping master thesis at the CES 2012 (Las Vegas)

Fingerprints strikes a deal with Tier 1

Signal Processing Devices AB

AnaCatum Design AB

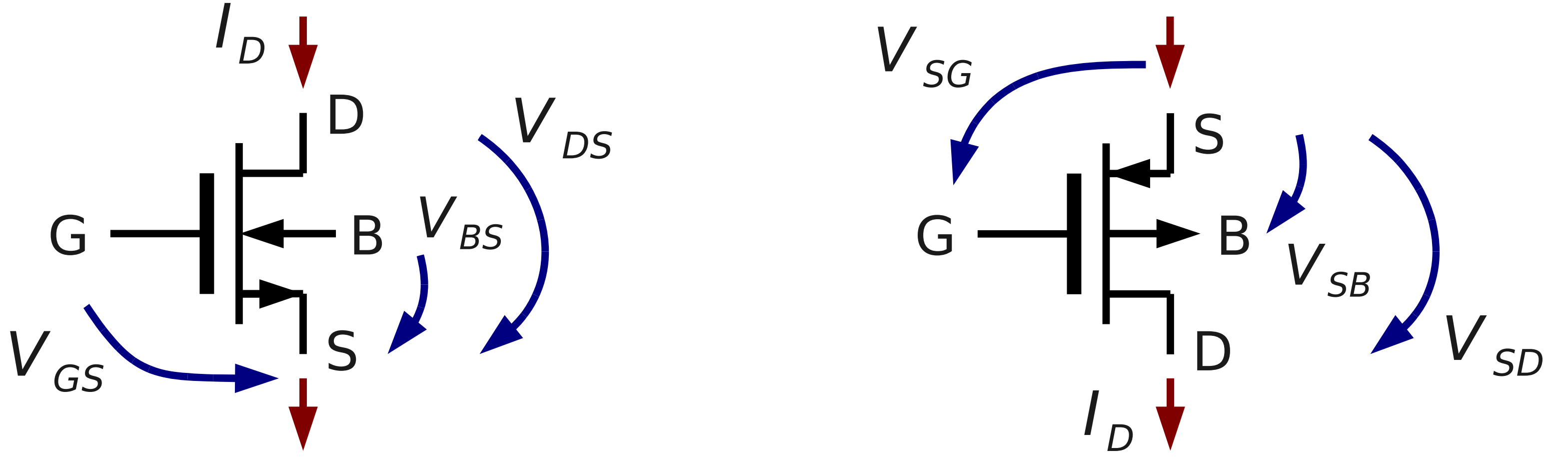
... and many, many more ...

Zzzzzzz, zzzz - get to the point!

MOS transistor

I hate semiconductor physics ...

... for me, it is about a couple of symbols and the formulas related to them



(a) NMOS (b) PMOS

The regions

Subthreshold (cut-off)	Linear (low gain)	Saturation (high gain)
$I \approx 0$	$I \approx \alpha \cdot \left(2 V_{eff} V_{ds} - V_{ds}^2 \right)$	$I \approx \alpha V_{eff}^2$
$V_{eff} < 0$	$V_{eff} > 0$, $V_{ds} < V_{eff}$	$V_{eff} > 0$, $V_{ds} > V_{eff}$

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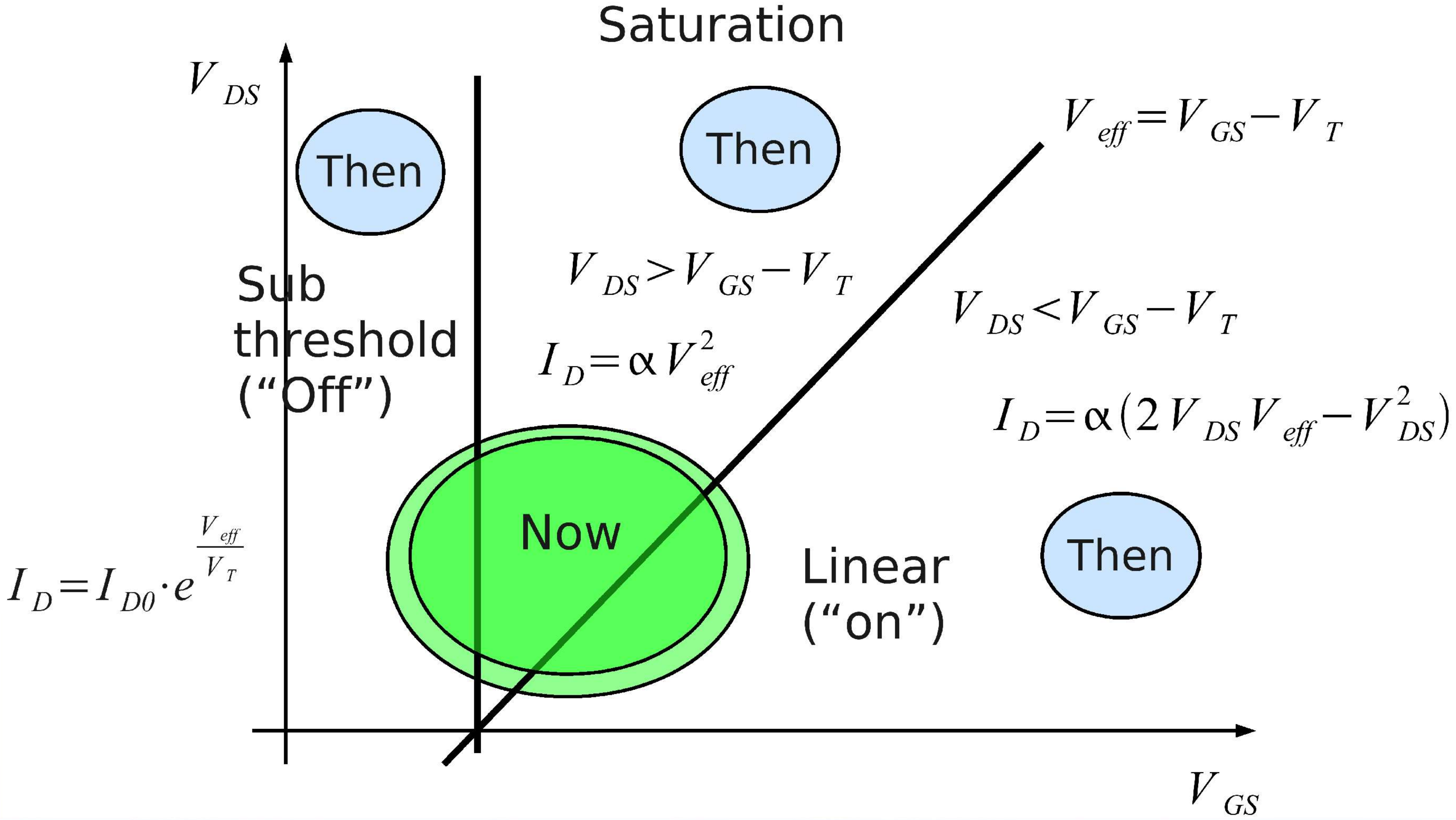
The regions, cont'd



The second-order effects

Subthreshold

$$I \approx I_{D0} \cdot e^{\frac{V_{eff}}{kT/q}}$$

Linear

$$I \approx \alpha \cdot \left(2 V_{eff} V_{ds} - V_{ds}^2\right)$$

Saturation

$$I \approx \alpha V_{eff}^2 \cdot \left(1 + \frac{V_{ds}}{V_\theta}\right)$$

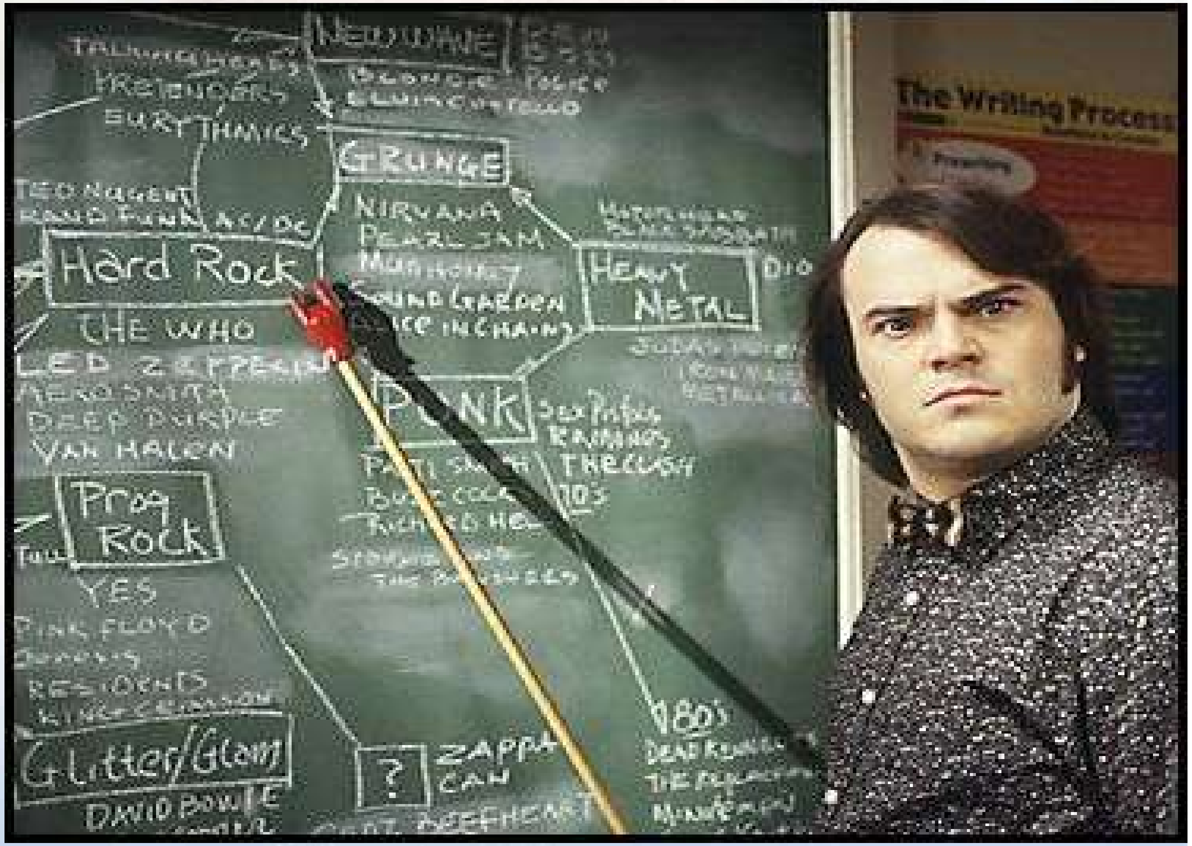
$$V_T = V_{T0} + \gamma \cdot \left(\sqrt{2\Phi_F - V_{BS}} - \sqrt{2\Phi_F}\right)$$ and $$V_\theta = 1/\lambda$$

The transistor in context, the common-source

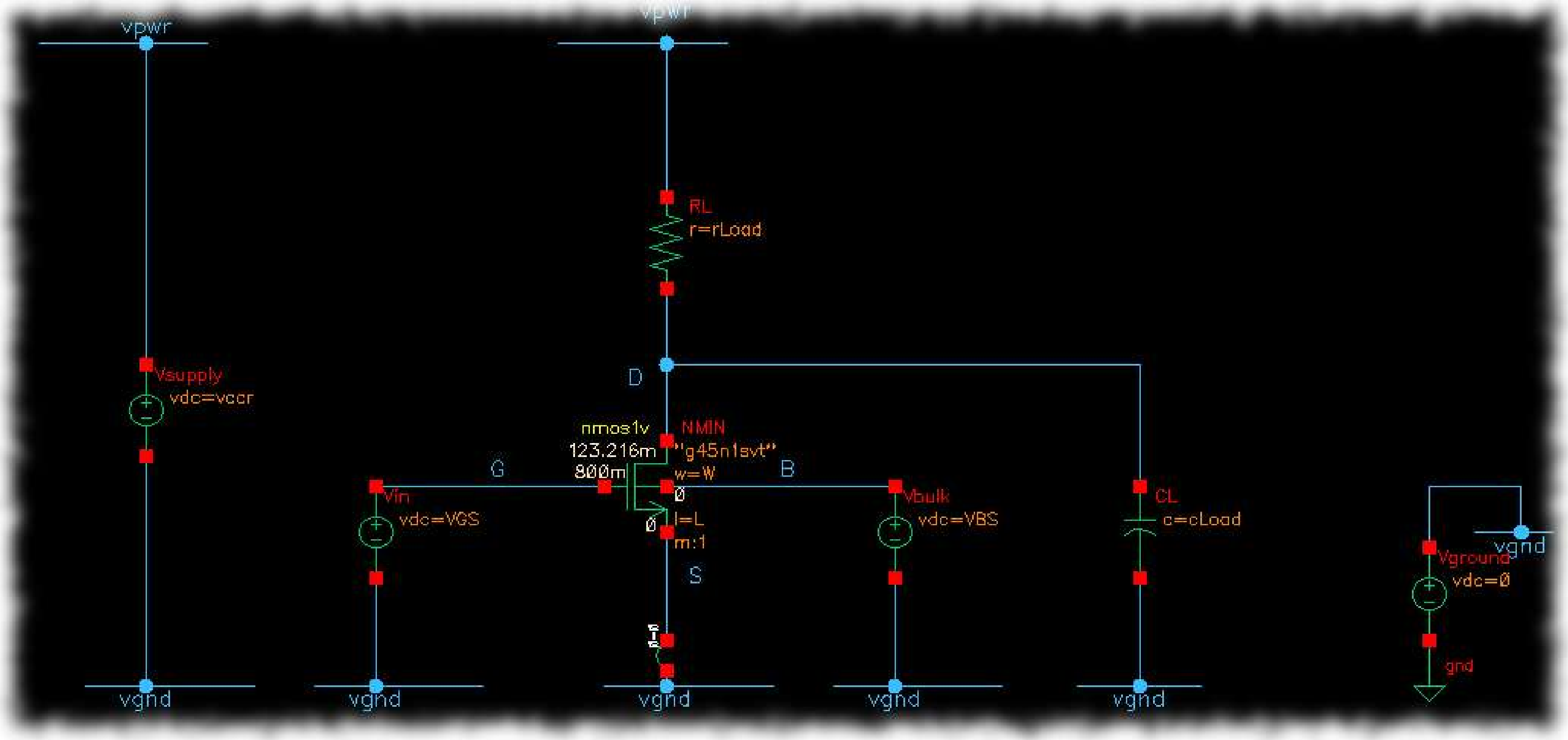
The circuit

The large-signal scenario

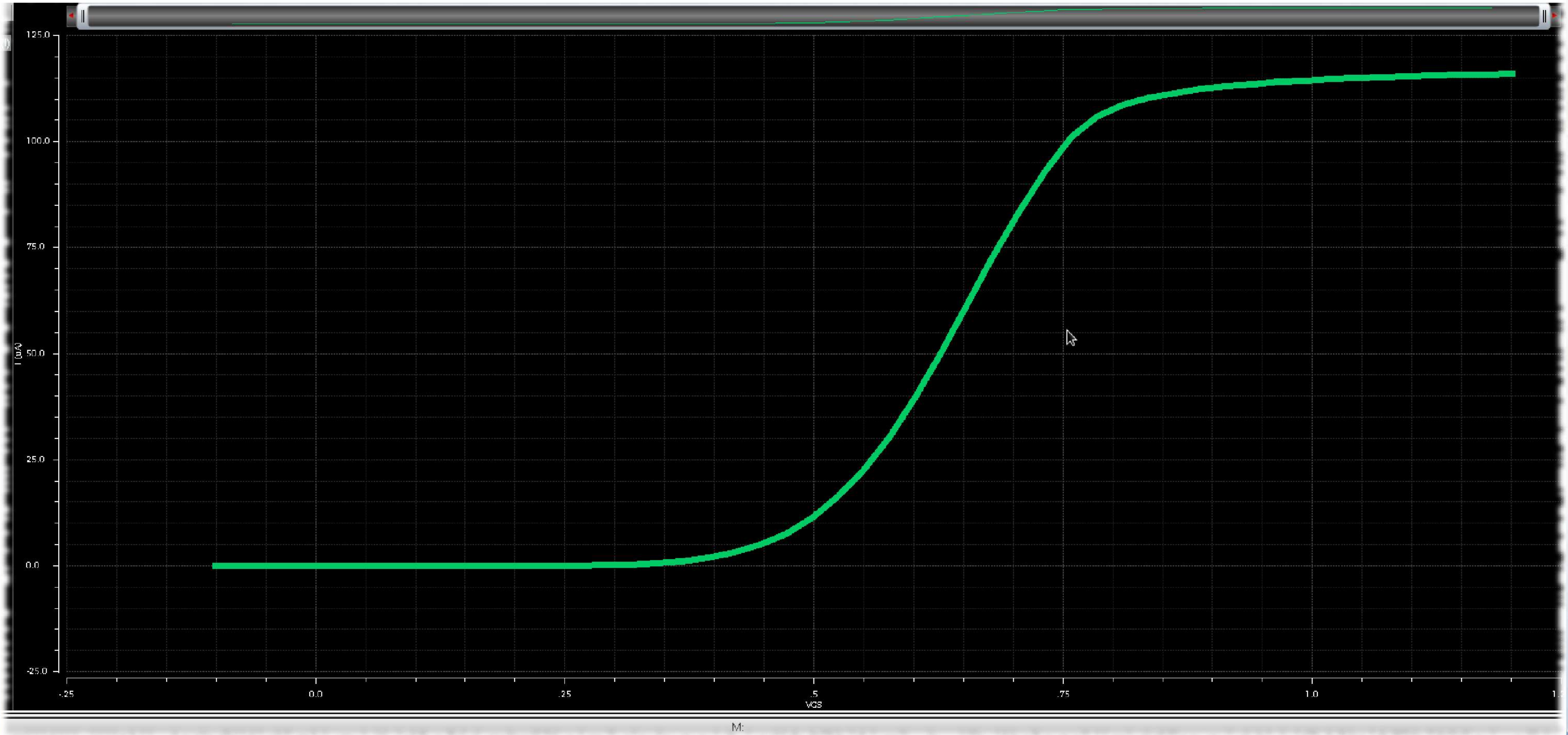
The small-signal scenario



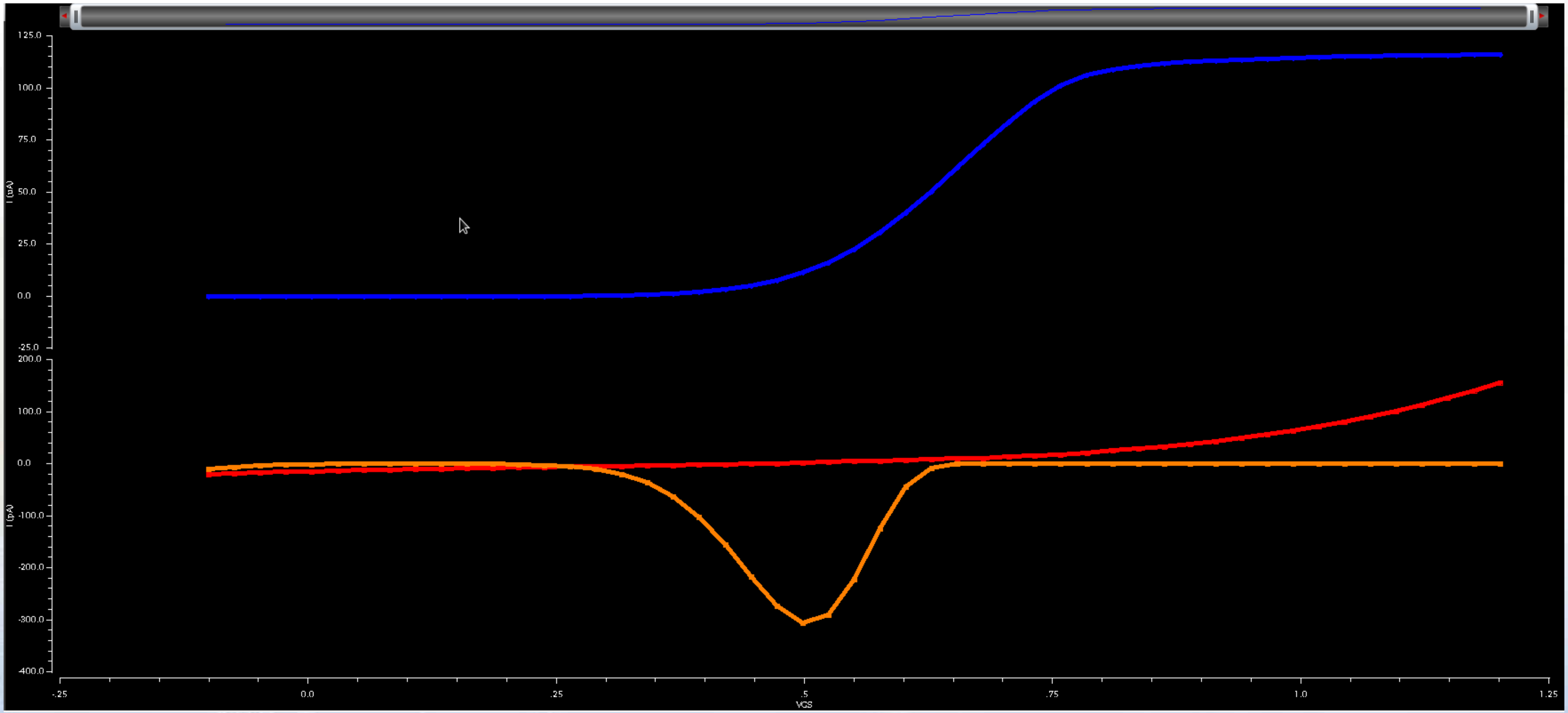
A simple testbench



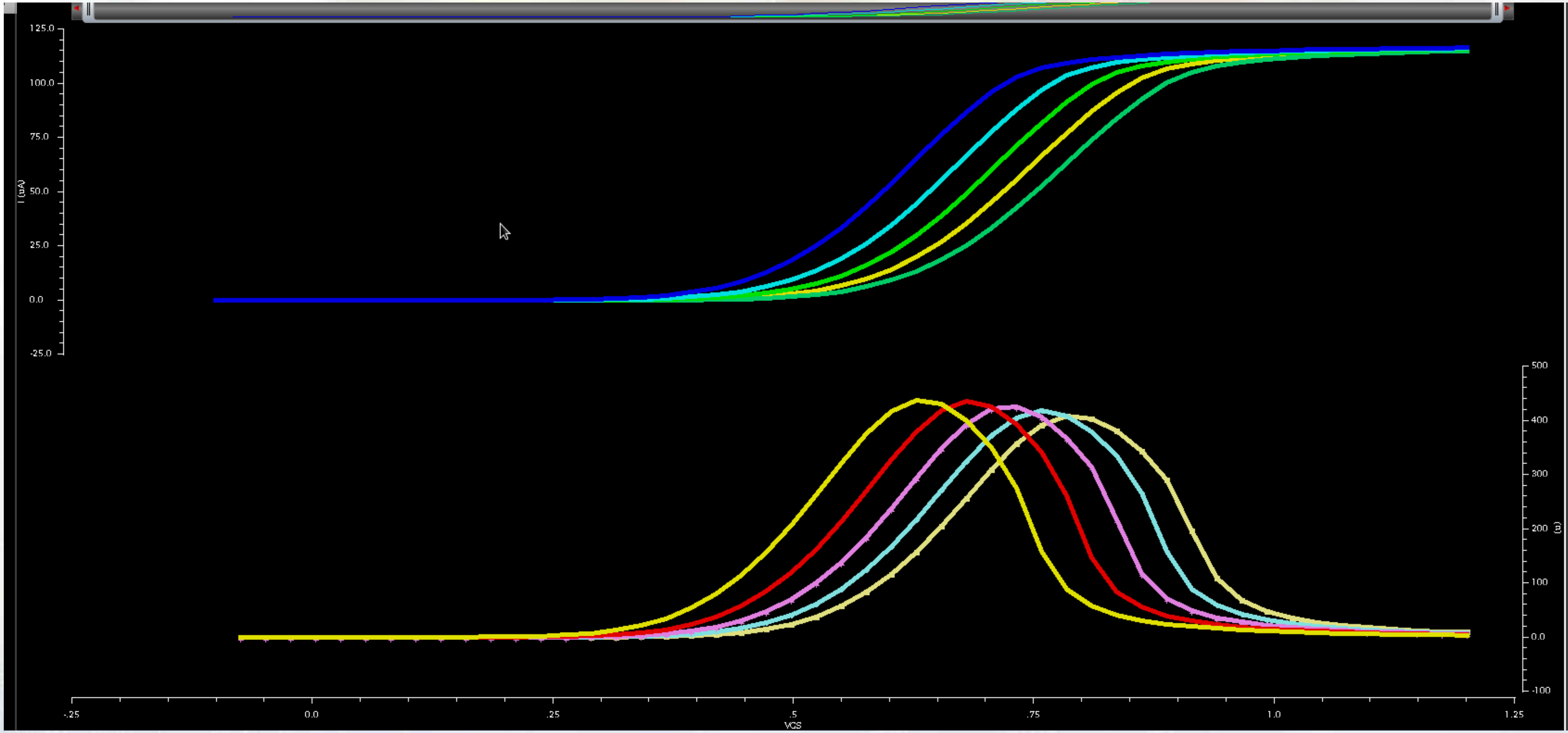
Simulation results, drain current



The second order effects



The second-order effects, cont'd



The derivative (lower graph) is the DC gain. The peak is reduced.

Transistors compiled

Expression	Cut-off	Linear	Saturation
g_m	$\dfrac{\kappa I_D}{kT/q}$	$2\alpha v_{ds}$	$\dfrac{2I_D}{v_{eff}}$ $2\sqrt{\alpha I_D}$
g_{mbs}	$g_m \cdot \dfrac{1-\kappa}{\kappa}$	$g_m \cdot \dfrac{\gamma}{2\sqrt{V_{SB}+2\phi_F}}$	$g_m \cdot \dfrac{\gamma}{2\sqrt{V_{SB}+2\phi_F}}$
g_{ds}	λI_D	$2\alpha\left(v_{eff}-v_{ds}\right)$	λI_D

Where is the gain highest?

Transistors compiled, cont'd

Expression	**Cut-off**	**Linear**	**Saturation**
$A=\frac{g_m}{g_{ds}}$	$\frac{\kappa\cdot q}{\lambda\cdot k\,T}$	$\frac{v_{ds}}{v_{eff}-v_{ds}}$	$\frac{2}{\lambda\cdot v_{eff}}$ $\frac{2\sqrt{\alpha}}{\lambda\sqrt{I_D}}$

What can you spot in this picture?

What did we do today?

Introduction to the course

Projects, labs, quizzes, exam, etc.

The transistor

Operating regions

First amplifier and parameters

Large vs small-signal

What will we do next time?

Further work on the analog building blocks

- Common-source, common-drain, common-gate
- Active vs passive load

Other "simple" analog building blocks

- Current mirrors

Mismatch

- And other things related to that