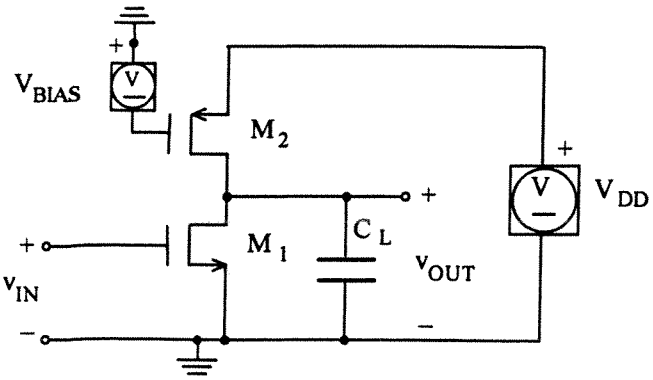
PROPERTIES BASIC AMPLIFIERS

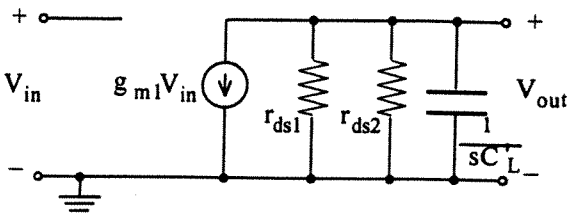
	COMMON SOURCE (CS)	COMMON DRAIN (CD)	COMMON GATE (CG)	CMOS INVERTER (CI)
Voltage-gain	**high (inv.)**	**low (<1) (non-inv.)**	**high (non- inv.)**	**high (inv.)**
Output resistance	**high**	**low**	**high**	**high**
Input resistance	**high**	**high**	**low**	**high**
Application areas	**inp.stage OP**	**outp.stage OP**	**low-resistance inp.stage (signal from transmission line**	**uncommon sensitive hard to design**

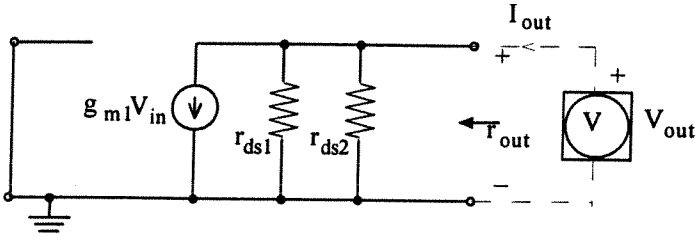
	CS	CD	CG	CI
A_o	$-\frac{g_{m1}}{g_{out}}$	$\frac{g_m}{g_{out}} \approx 1$	$\frac{g_{m1}+g_{b1}}{g_{out}} \approx \frac{g_{m1}}{g_{out}}$	$-\frac{g_{m1}+g_{m2}}{g_{out}}$
p_1	$-\frac{g_{out}}{C_L'}$	$-\frac{g_{out}}{C_L'}$	$-\frac{g_{out}}{C_L'}$	$-\frac{g_{out}}{C_L'}$
ω_u	$\frac{g_{m1}}{C_L'}$	$\frac{g_{m1}}{C_L'}$	$\approx \frac{g_{m1}}{C_L'}$	$\frac{g_{m1}+g_{m2}}{C_L'}$
g_{out}	$g_{ds1}+g_{ds2}$	$g_{m1}+g_{b1}+g_{ds1}+g_{ds2}$	$g_{ds1}+g_{ds2}$	$g_{ds1}+g_{ds2}$
g_{in}	0	0	$g_{m1}.\frac{1}{1+\frac{g_{ds1}}{g_{ds2}}}$	0

COMMON SOURCE AMPLIFIER

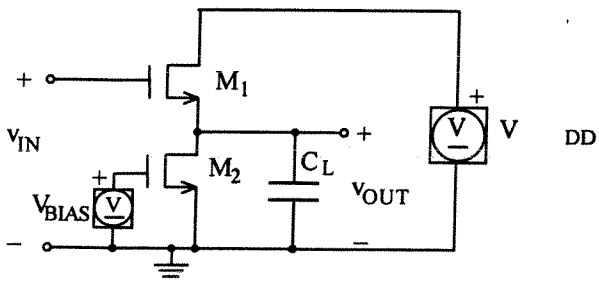


SMALL-SIGNAL EQUIVALENT CIRCUIT (SSEC)

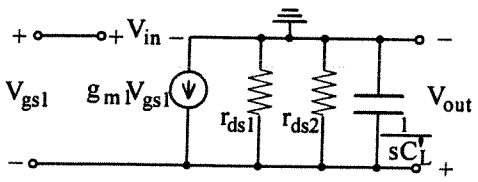


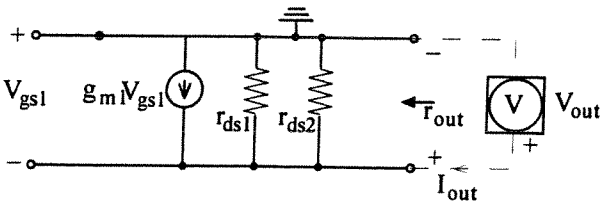


COMMON DRAIN AMPLIFIER

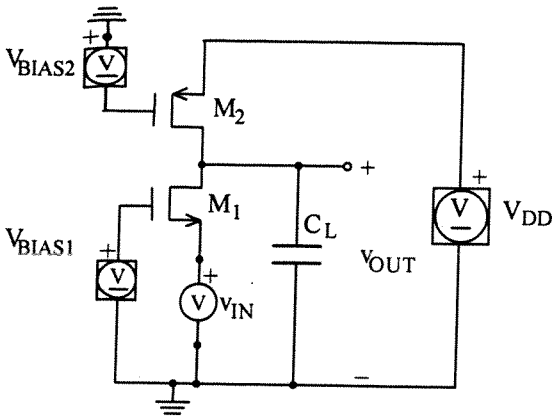


SMALL-SIGNAL EQUIVALENT CIRCUIT (SSEC)

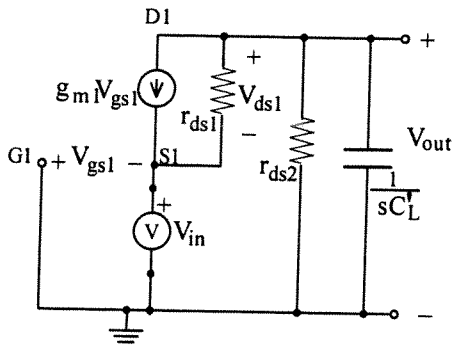


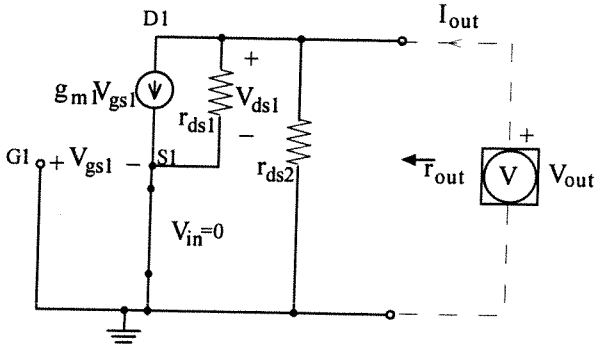


COMMON GATE AMPLIFIER

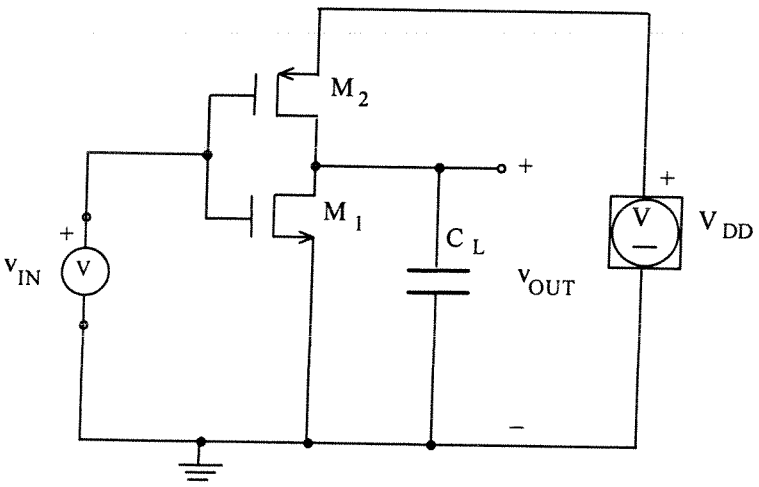


SMALL-SIGNAL EQUIVALENT CIRCUIT (SSEC)

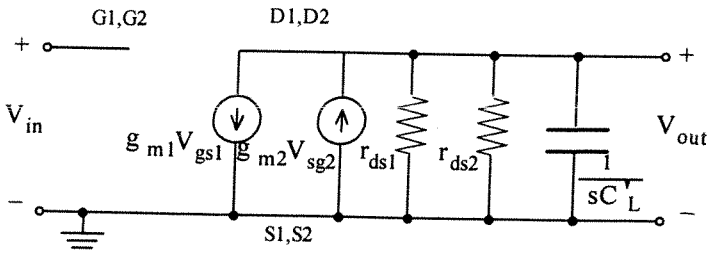




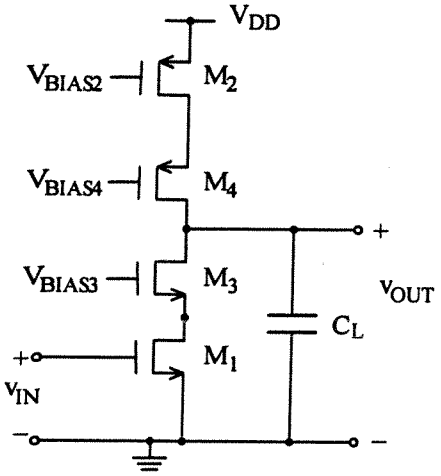
CMOS-INVERTER



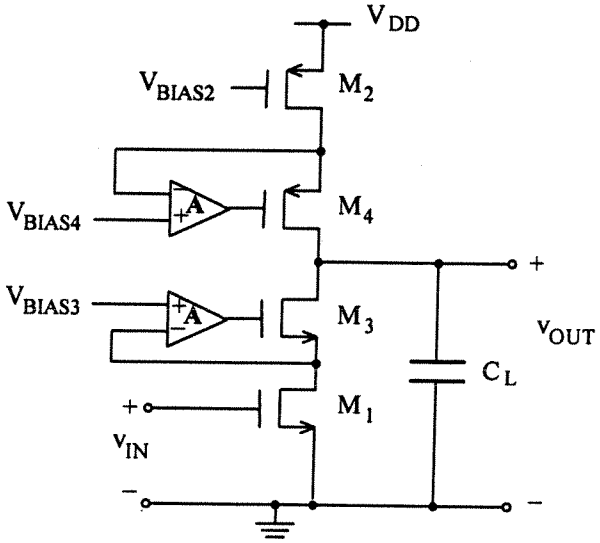
SMALL-SIGNAL EQUIVALENT CIRCUIT (SSEC)



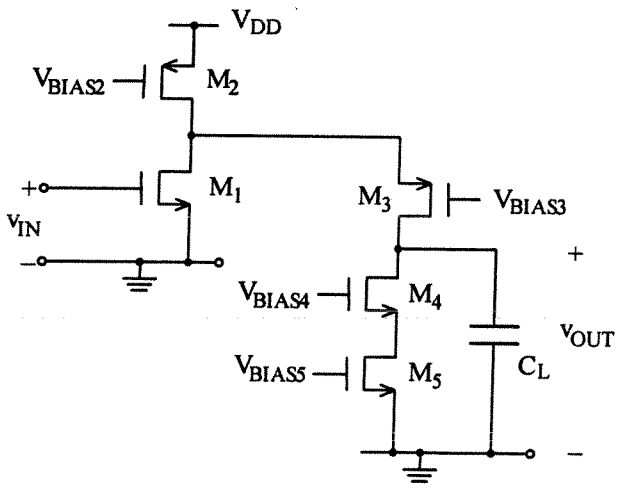
COMMON SOURCE AMPLIFIER WITH CASCODE



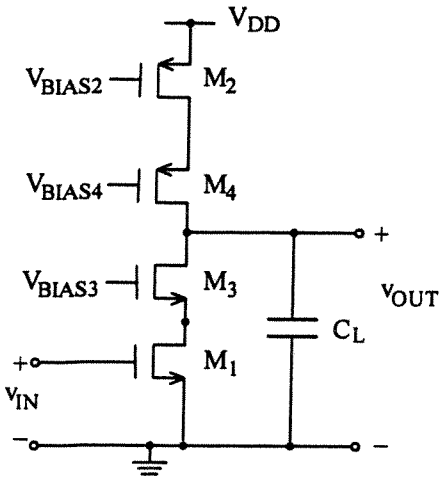
COMMON SOURCE AMPLIFIER WITH CASCODE. EXTRA BIAS



COMMON SOURCE AMPLIFIER WITH FOLDED CASCODE

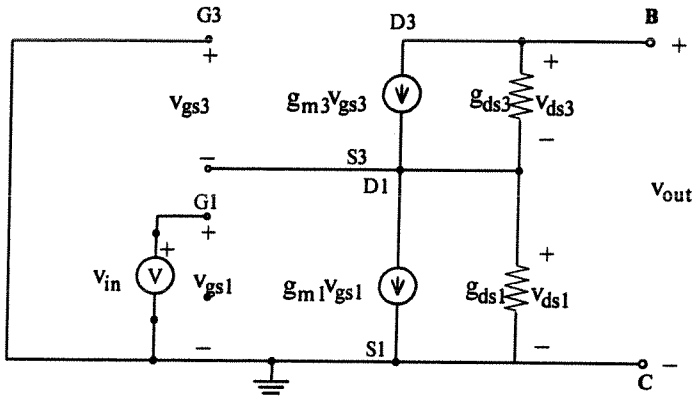


COMMON SOURCE AMPLIFIER WITH CASCODE



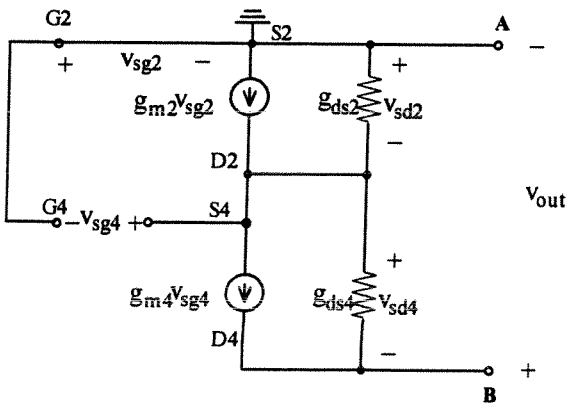
SSEC

NMOS-part

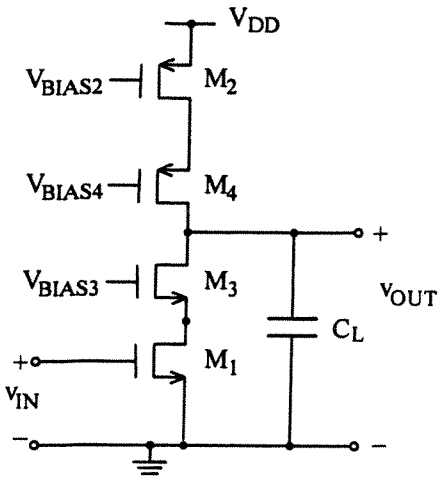


SSEC

PMOS-part

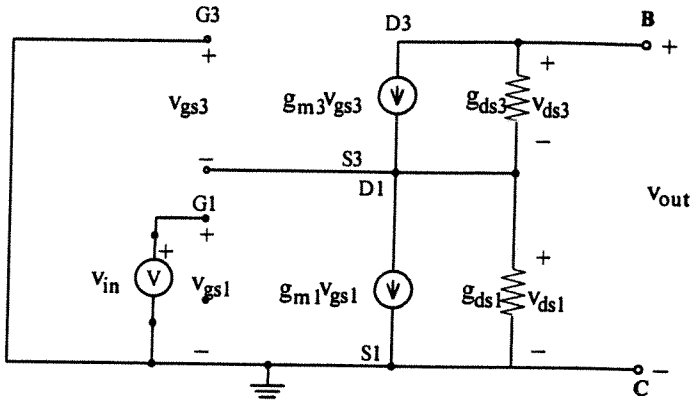


COMMON SOURCE AMPLIFIER
WITH CASCODE



SSEC

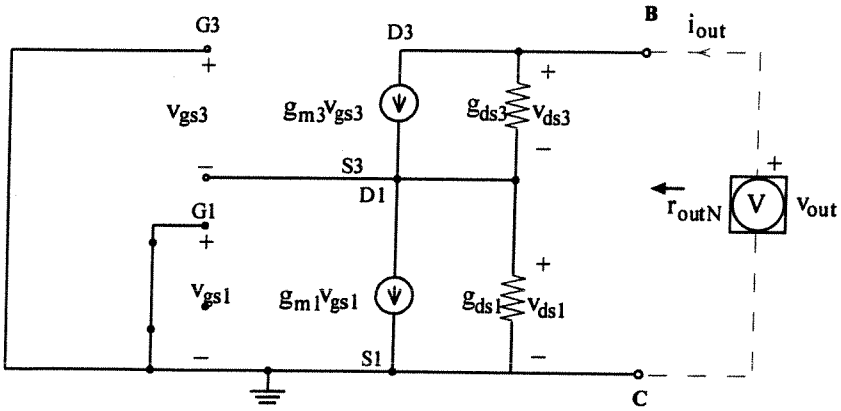
NMOS-part



Dertermine r_{out}

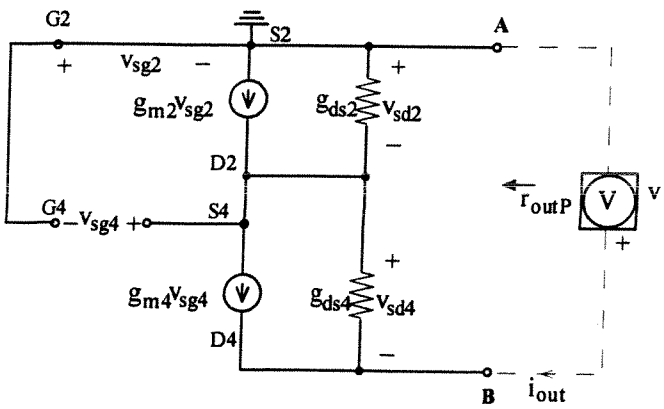
SSEC

NMOS-part

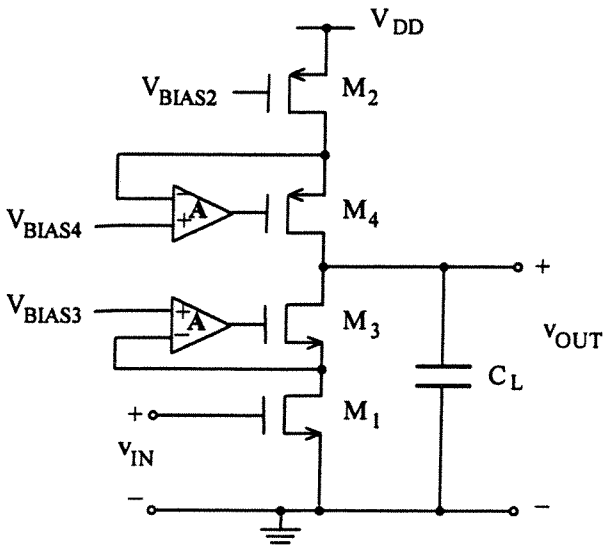


SSEC

PMOS-part



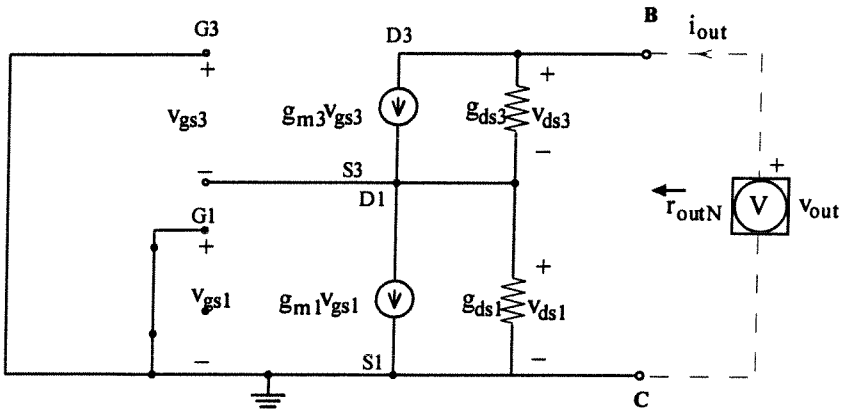
COMMON SOURCE AMPLIFIER WITH CASCODE. EXTRA BIAS



Determine r_{out}

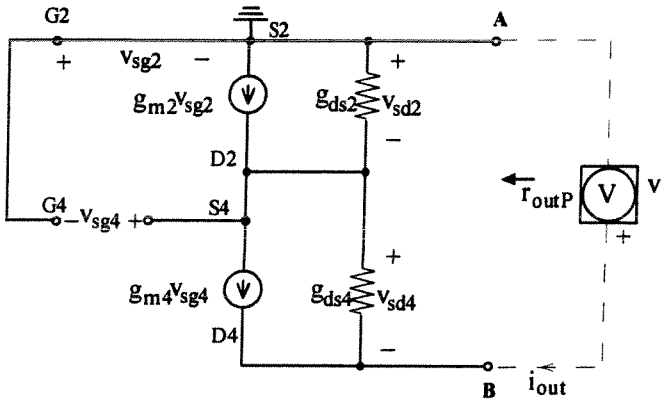
SSEC

NMOS-part

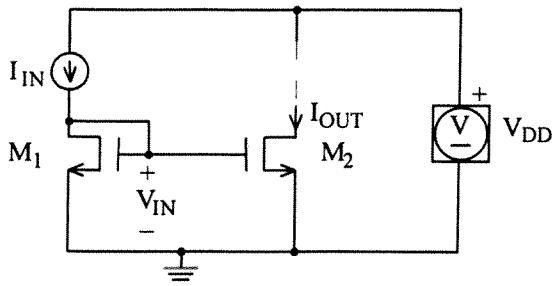


SSEC

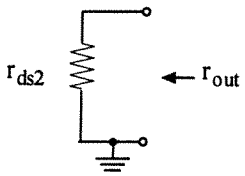
PMOS-part



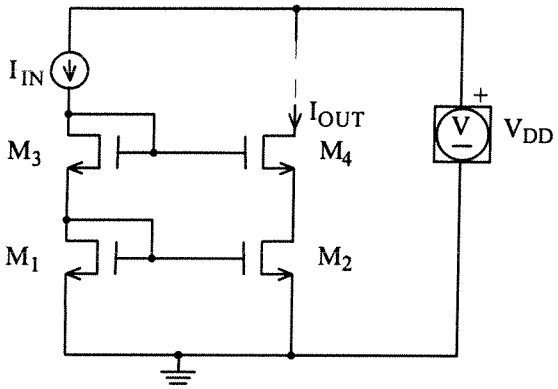
CURRENT MIRROR



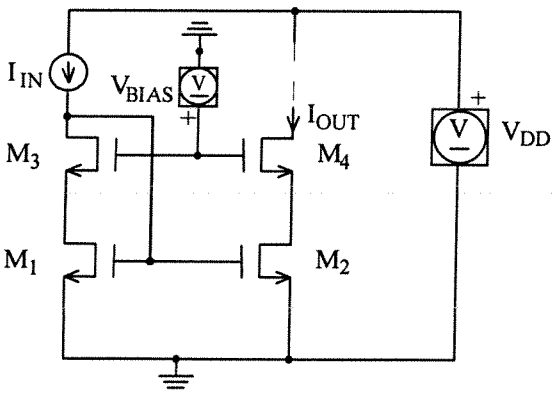
SMALL SIGNAL EQUIVALENT CIRCUIT (SSEC)

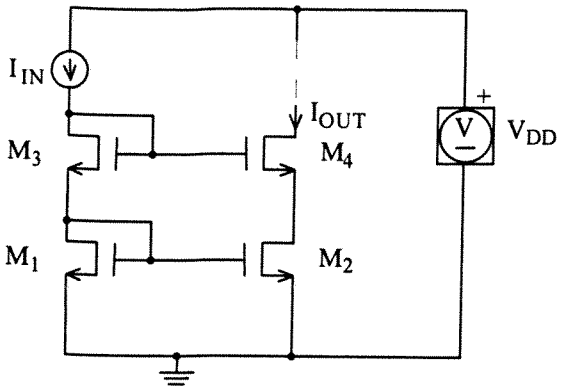


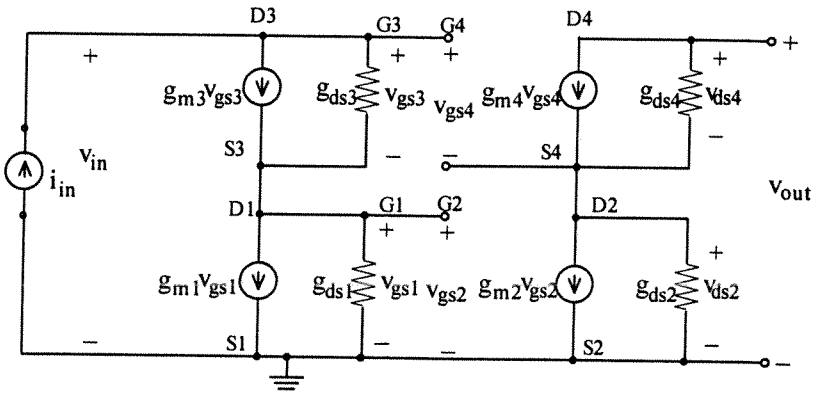
CASCODE CURRENT MIRROR



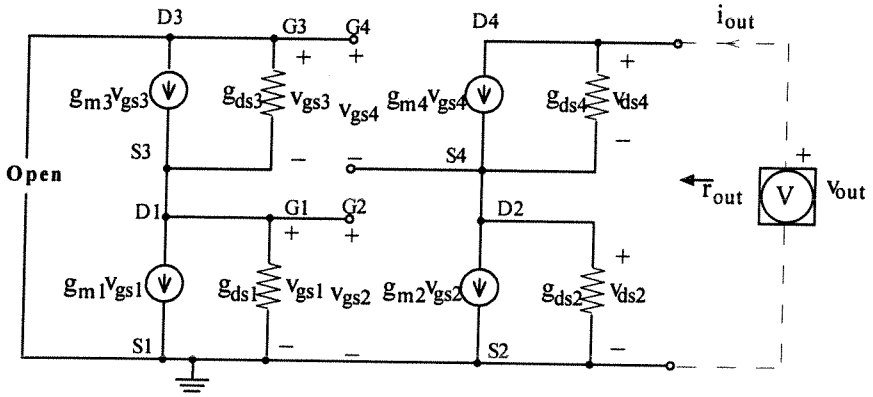
WIDE-SWING CURRENT MIRROR

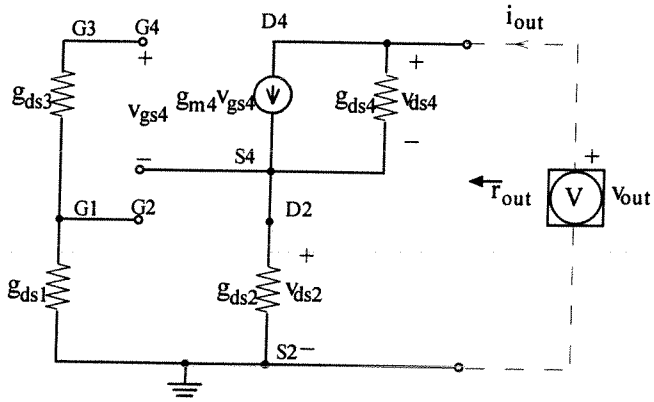




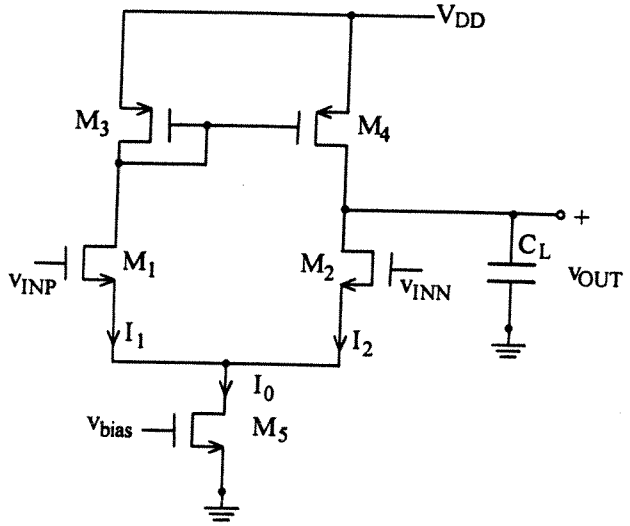


Determine r_{out}





DIFFERENTIAL GAINSTAGE **(Large signal analysis)**



Assumptions: 1) All transistors saturated
2) $V_{INP} = V_{INN} = V_{IN}$ (COMMON MODE)

CMR (Common Mode Range) = $[V_{IN}\min, V_{IN}\max]$
OR (Output Range) = $[V_{OUT}\min, V_{OUT}\max]$

$$V_{IN}\min = V_{DS5} + V_{GS1} = V_{eff5} + V_{eff1} + V_{t1} = \sqrt{\frac{I_0}{\alpha_5}} + \sqrt{\frac{I_0/2}{\alpha_1}} + V_{t1}$$

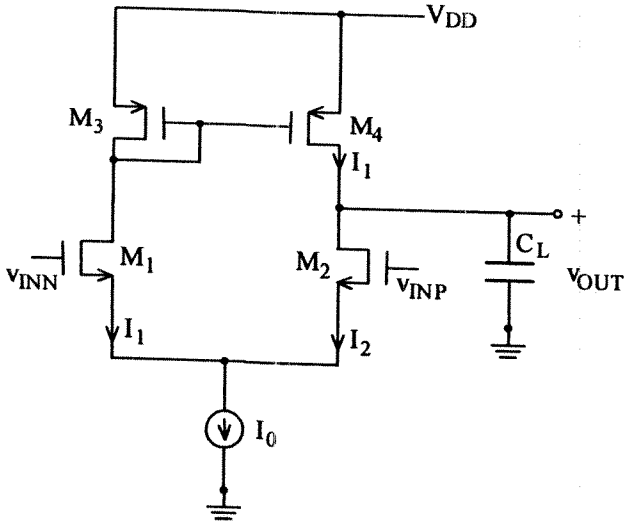
$$V_{IN}\max = V_{DD} - V_{SG3} - V_{DS1} + V_{GS1} = V_{DD} - V_{eff3} - V_{t3} - V_{eff1} + V_{eff1} + V_{t1} =$$

$$= V_{DD} - \sqrt{\frac{I_0/2}{\alpha_3}} - V_{t3} + V_{t1}$$

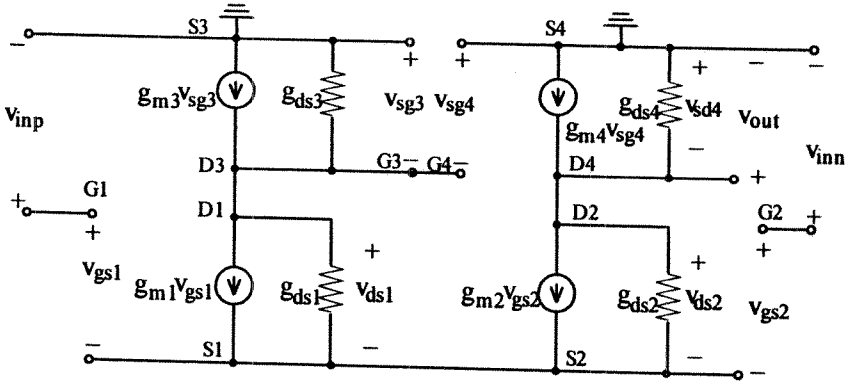
$$V_{OUT}\min = V_{DS5} + V_{DS2} = V_{eff5} + V_{eff1} = \sqrt{\frac{I_0}{\alpha_5}} + \sqrt{\frac{I_0/2}{\alpha_2}}$$

$$V_{OUT}\max = V_{DD} - V_{SD4} = V_{DD} - V_{eff4} = V_{DD} - \sqrt{\frac{I_0/2}{\alpha_4}}$$

DIFFERENTIAL GAINSTAGE



SSEC



Determine $\frac{v_{out}}{v_{inp}-v_{inn}}$ for differential gain stage.

1) Introduce variables v_x (at node x, i.e. node D1,D3) and v_y (at node y, i.e. node S1,S2).

2) Express v_{gs1}, v_{gs2}, v_{sg3} $(=v_{sd3})$, v_{sg4}, v_{ds1}, v_{ds2}, v_{sd4} in v_{inp}, v_{inn}, v_x, v_y and v_{out}.

$$v_{gs1} = v_{g1} - v_{s1} = v_{inp} - v_y \qquad v_{ds1} = v_x - v_y$$
$$v_{gs2} = v_{g2} - v_{s2} = v_{inn} - v_y \qquad v_{ds2} = v_{out} - v_y$$
$$v_{sg3} = -v_x \qquad v_{sd3} = v_{sg3} = -v_x$$
$$v_{sg4} = v_{sg3} = -v_x \qquad v_{sd4} = -v_{out}$$

3) Nodal analysis on node x, node out and gnd.

Node x: $g_{m3}(-v_x) - g_{ds3}v_x - g_{m1}(v_{inp} - v_y) - g_{ds1}(v_x - v_y) = 0$ (1)

Node out: $g_{m4}(-v_x) - g_{ds4}v_{out} - g_{m2}(v_{inn} - v_y) - g_{ds2}(v_{out} - v_y) = 0$ (2)

gnd.: $-g_{m3}(-v_x) + g_{ds3}v_x - g_{m4}(-v_x) + g_{ds4}v_{out} = 0$ (3)

$$(3) \Rightarrow v_x = \frac{-g_{ds4}v_{out}}{g_{m3} + g_{m4} + g_{ds3}} \quad (4)$$

$$(1),(2) \Rightarrow \begin{array}{l} v_x(g_{m3} - g_{m4} + g_{ds3}) - g_{ds4}v_{out} + g_{m1}v_{inp} - g_{m2}v_{inn} - v_y(g_{m1} - g_{m2}) \\ + g_{ds1}v_x - g_{ds2}v_{out} - v_y(g_{ds1} - g_{ds2}) = 0 \end{array} \quad (5)$$

4) Assume $g_{ds1} = g_{ds2}$, $g_{ds3} = g_{ds4}$, $g_{m1} = g_{m2}$ and $g_{m3} = g_{m4}$

$$(5) \Rightarrow v_x g_{ds4} - g_{ds4}v_{out} + g_{m1}(v_{inp} - v_{inn}) + g_{ds2}(v_x - v_{out}) = 0 \quad (6)$$

$$(4),(6) \Rightarrow g_{m1}(v_{inp} - v_{inn}) = v_{out}\left(g_{ds2} + \frac{g_{ds2}g_{ds4}}{g_{m3} + g_{m4} + g_{ds3}} + g_{ds4} + \frac{g_{ds4}^2}{g_{m3} + g_{m4} + g_{ds3}}\right) \quad (7)$$

But $g_{ds3} = g_{ds4}$ and $g_{m3} = g_{m4}$ which gives:

$$(7) \Rightarrow g_{m1}(v_{inp} - v_{inn}) = v_{out}\left(g_{ds2} + \frac{g_{ds2}g_{ds4}}{2g_{m4} + g_{ds4}} + g_{ds4} + \frac{g_{ds4}^2}{2g_{m4} + g_{ds4}}\right) \quad (8)$$

$$(8) \Rightarrow g_{m1}(v_{inp} - v_{inn}) = v_{out}g_{ds2}\left(1 + \frac{g_{ds4}}{2g_{m4} + g_{ds4}}\right) + v_{out}g_{ds4}\left(1 + \frac{g_{ds4}}{2g_{m4} + g_{ds4}}\right) \quad (9)$$

$$(9) \Rightarrow g_{m1}(v_{inp} - v_{inn}) = v_{out}\left(1 + \frac{g_{ds4}}{2g_{m4} + g_{ds4}}\right)(g_{ds2} + g_{ds4}) \quad (10)$$

$$(10) \Rightarrow g_{m1}(v_{inp} - v_{inn}) = v_{out}\left(\frac{2g_{m4} + 2g_{ds4}}{2g_{m4} + g_{ds4}}\right)(g_{ds2} + g_{ds4}) \quad (11)$$

$$(11) \Rightarrow \frac{v_{out}}{v_{inp} - v_{inn}} = \frac{g_{m1}(2g_{m4} + g_{ds4})}{2(g_{ds2} + g_{ds4})(g_{m4} + g_{ds4})} \approx \frac{g_{m1}}{g_{ds2} + g_{ds4}}$$

PERFORMANCE MEASURES FOR DIFFERENTIAL GAIN STAGE

LARGE SIGNAL ANALYSIS:

- Common Mode Range, $CMR = [V_{inmin}, V_{inmax}]$
- Output range, $OR = [V_{outmin}, V_{outmax}]$
- Slew Rate, $SR = max\left\{\frac{dv_{out}}{dt}\right\}$

SMALL SIGNAL ANALYSIS:

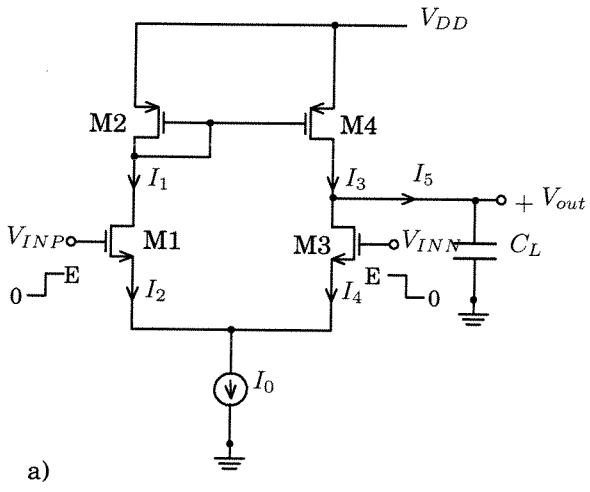
- Common Mode Rejection Ratio, $CMRR = 20 \cdot^{10} \log \frac{A_d}{A_{cm}}$
- Power Supply Rejection Ratio +, $PSRR_+ = 20 \cdot^{10} \log \frac{A_d}{A_{Vdd \rightarrow V_{out}}}$
- Power Supply Rejection Ratio -, $PSRR_- = 20 \cdot^{10} \log \frac{A_d}{A_{gnd \rightarrow V_{out}}}$

- A_d=Amplification for differential input signals
- A_{cm}=Amplification for common-mode input signals
- $A_{Vdd \rightarrow V_{out}}$=Amplification for variations in $+V_{dd}$ from V_{dd} to V_{out}
- $A_{gnd \rightarrow V_{out}}$=Amplification for variations in ground from ground to V_{out}

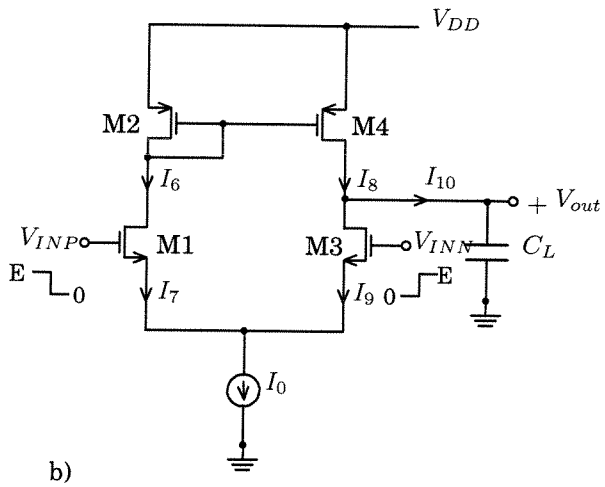
To determine $A_{Vdd \rightarrow V_{out}}$ set the AC-input signal to zero and introduce an AC-source at $V_{dd}+$. $A_{gnd \rightarrow V_{out}}$ determins in the same way by setting the AC-input signal to zero and introduce an AC-source at $V_{dd}-$ (ground).

DETERMINATION OF SLEW-RATE

To determine Slew-Rate (SR) for the differential gain-stage below, apply a square-pulse on V_{INP} and an inverted square-pulse on V_{INN}. Figure a) gives phase 1, when V_{INP} grows instantaneously from 0 to E and V_{INN} at the same time instantaneously goes from E to 0. Figure b) shows phase II that starts with V_{INP} instantaneously decreasing from E to 0 and V_{INN} instantaneously increasing from 0 to E.
E is larger than V_{tn} ($E > V_{tn}$). Transistors M1 and M3 are identical as well as M2 and M4.



a)



b)

Phase I:
- $V_{INP} = +E, V_{INN} = 0 \Rightarrow$ M1 conducts and M3 blocks.
- M3 blocks $\Rightarrow I_4 = 0$
  M1 conducts $\Rightarrow I_1 = I_2 = I_0$
- M2 and M4 is a current mirror and as M2 and M4 are identical $I_3 = I_1 = I_0$
- M3 blocks ($I_4 = 0$) $\Rightarrow I_5 = I_3 = I_0$

Phase II:
- $V_{INP} = 0, V_{INN} = +E \Rightarrow$ M1 blocks and M3 conducts.
- M1 blocks $\Rightarrow I_6 = I_7 = 0$
- M2 and M4 is a current mirror $\Rightarrow I_8 = I_6 = 0$
- M3 conducts $\Rightarrow I_9 = I_0$
- $I_8 = 0$ and $I_9 = I_0 \Rightarrow I_{10} = -I_9 = -I_0$

$$\text{Definition: Slew-Rate (SR)} = \max \frac{dv_{out}(t)}{dt}$$

For capacitor C_L:

$$i_{CL}(t) = C_L \frac{dv_{CL}(t)}{dt} = C_L \frac{dv_{out}(t)}{dt} \Rightarrow \frac{dv_{out}}{dt} = \frac{i_{CL}(t)}{C_L}$$

Thus, maximum value of $\frac{dv_{out}(t)}{dt}$ obtains for maximum value of $i_{CL}(t)$, which has been shown above to be I_0.

$$\textbf{I.e. Slew-Rate} = \underline{\underline{\frac{I_0}{C_L}}}$$