TSEK37

Analog CMOS Integrated Circuits

Examination (TEN1)

Time:	1 April 2016 at 8.00 - 12.00
Place:	G32
Responsible teacher:	Martin Nielsen-Lönn, ISY, 070-361 52 44 (martin.nielsen.lonn@liu.se)
	Will visit exam location at 9 and 11.
Number of tasks:	6
Number of pages:	6
Allowed aids:	Calculator, dictionary
Total points:	20
Notes:	Remember to indicate the steps taken when solving problems.
	Please start each new problem at the top of a page!
	Only use one side of each paper!
Exam presentation:	8 April 2016 at 12:00-13:00 in 3D:535, B-building

Grade	**Points**
U	<8
3	8 - <12
4	12 - <16
5	16 - 20

Questions

1) Consider the circuit shown in Fig. 1.

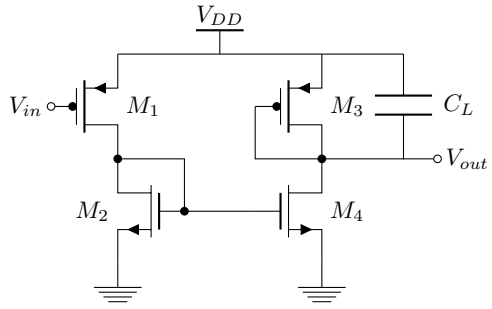

Figure 1: Schematic of a single-ended amplifier.

(a) Draw the equivalent small-signal model and derive the expression for the transfer function and from that transfer function identify the DC voltage gain and pole(s). Neglect channel-length modulation and body effect ($\lambda = 0$, $\gamma = 0$). Ignore all parasitic capacitances. (3)

(b) Assume that a parasitic pole ω_{p2} appears in the circuit shown in Fig. 1 and the unity-gain frequency $\omega_{ug} = 20$ krad/s, the dominant pole $\omega_{p1} = 2$ krad/s and the phase margin PM $= 60°$. Determine the value of this non-dominant pole ω_{p2} caused by parasitics. Assume that the poles are well separated. (1)

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2) Consider the fully differential amplifier shown in Fig. 2. The amplifier is completely symmetric. Neglect body effect ($\gamma = 0$). However, channel-length modulation must be considered ($\lambda \neq 0$). The parasitic capacitance C_{gs} of the MOSFETs at nodes X, Y and the load capacitance C_L must be considered. Ignore other parasitic capacitances. Assume that $g_m \gg g_{ds}$.

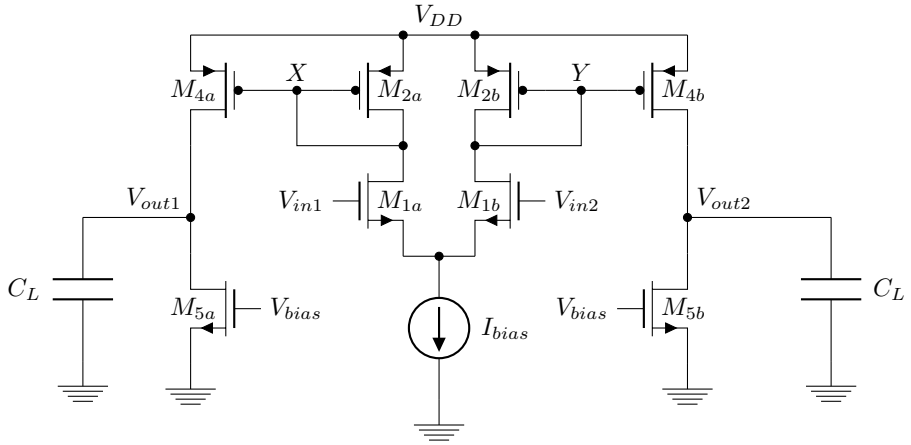

Figure 2: A fully differential amplifier.

(a) Draw the small-signal model of the amplifier shown in Fig. 2 and derive the transfer function. (2½)

(b) Derive the expressions for the DC gain, the two pole frequencies and the unity-gain frequency. It is assumed that the dominant pole is formed by the load capacitor C_L. (1)

(c) If the width of M_4 increases, how will this change the non-dominant pole and the unity-gain frequency? It is assumed that the dominant pole is formed by the load capacitor C_L. (½)

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3) In Fig. 3 a current mirror circuit is shown. The aim is to copy the reference current I_{ref} to I_{out}. This requires a high output impedance and preferably a low voltage headroom.

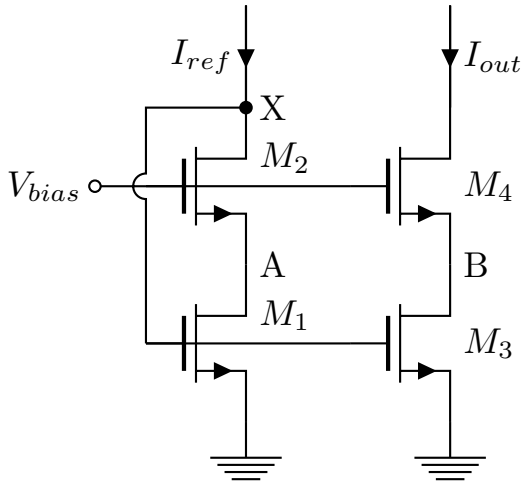

Figure 3: A wide-swing cascode current mirror.

(a) Derive the bounds for V_{bias} such that both M_1 and M_2 are in the saturation region. Give the answers in terms of V_{gs1}, V_{gs2}, V_{th1} and V_{th2}. (2)

(b) Using the lowest value for V_{bias} derived in part 1, determine the minimum allowable voltage at the output node to keep both M_3 and M_4 in the saturation region. Assume that $M_3 = M_1$ and $V_{gs4} = V_{gs2}$. Give the answer in terms of V_{gs3}, V_{gs4}, V_{th3} and V_{th4}. (1)

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4) Figure 4 shows a lossless interconnect circuit. At $t = 0$ the voltage step V_0 goes high and propagates a pulse through the circuit. Given the values below, calculate the voltage at nodes A, B and C at $t = 7$ ns. t_{d,Z_x} is the delay through transmission line Z_x. Assume that the inverters have a infinite (high) input impedance. (3)

$R_0 = 150\ \Omega$, $Z_0 = 150\ \Omega$, $Z_1 = 75\ \Omega$, $Z_2 = 50\ \Omega$, $t_{d,Z_0} = 2$ ns, $t_{d,Z_1} = 3$ ns and $t_{d,Z_2} = 4$ ns.

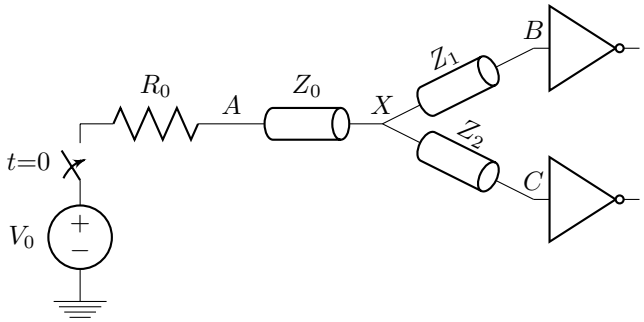

Figure 4: Transmission line circuit.

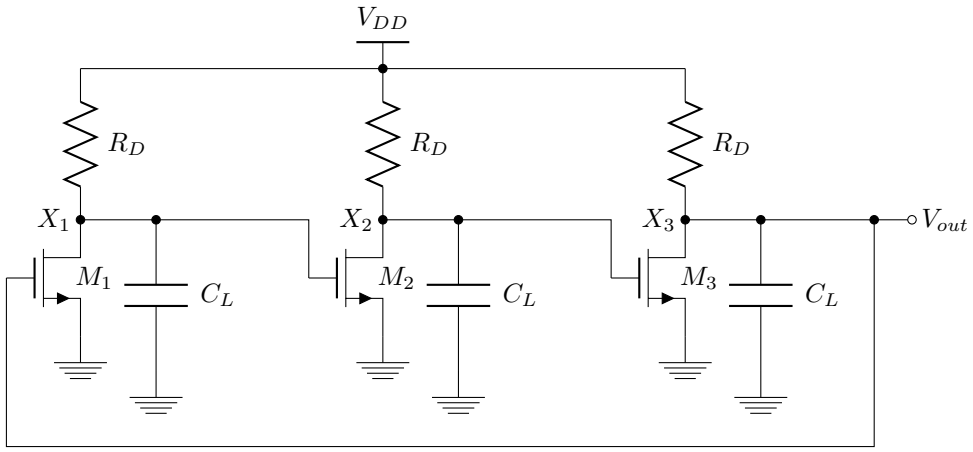

Figure 5: 3-stage ring oscillator

5) (a) In Fig. 5 a 3-stage ring oscillator is shown. What is the *maximum* phase of V_{out} this circuit can have when $\omega \to \infty$? Divide the phase shift into DC phase shift and frequency dependent phase shift. (1)

(b) Given the Barkhausen criteria, (2)

$$|H(j\omega_0)| \geq 1$$
$$\angle H(j\omega_0) = 180^\circ$$

and the pole frequency ω_p and DC-gain A_0 for each stage. At what frequency will the circuit oscillate? And what gain is required for each stage? Assume that all stages are equal.
Hint: $tan(60^\circ) = \sqrt{3}$.

(c) Derive the total transfer function for the system first in terms of DC-gain, A_0, and poles, ω_{p1} and then with the circuit components R_D, C_L, g_m and g_{ds}. Identify the DC-gain and pole location in the second transfer function. Assume that all stages are equal, that parasitic capacitances can be neglected and $1/g_{ds} >> R_D$. (1)

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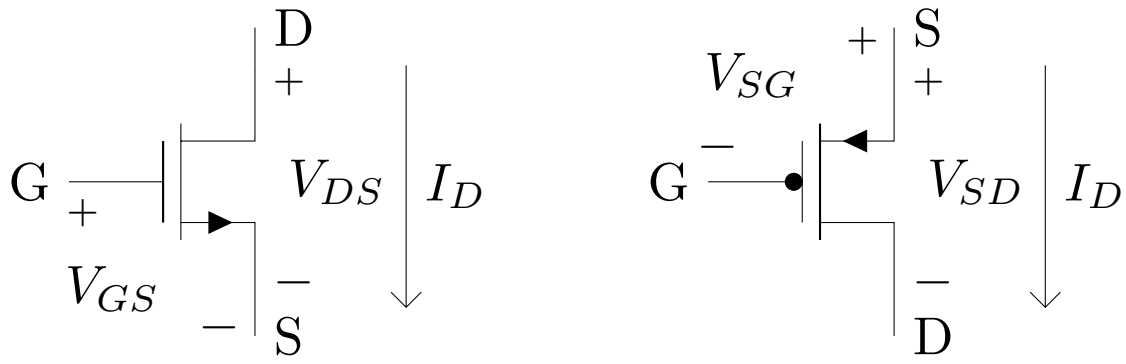
6) (a) An XOR gate is used as a phase dector in a DLL. Assume that the phase difference between the input and output of the DLL is 225°. Draw the input and output waveforms of the XOR (*DLL In*, *DLL Out* and *XOR Out*). Also calculate the average output voltage of the phase detector. Assume that the waveforms are ideal square waves with a swing between 0 V and 1 V. (1)

(b) A PLL type I can be used to multiply a frequency. Assume that the PLL is supposed to generate a frequency of 1 GHz from a 250 MHz clock. Draw the block diagram for this kind of PLL. (1)

Transistor equations



(a) NMOS (b) PMOS

NMOS

Cutoff $I_D = 0$ $(V_{GS} < V_{TN})$

Linear mode

$I_D = \mu_n C_{ox} \frac{W}{L} \left((V_{GS} - V_{TN}) V_{DS} - \frac{V_{DS}^2}{2} \right)$ $(V_{GS} > V_{TN})$ and $(V_{DS} < V_{GS} - V_{TN})$

Saturation mode

$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TN})^2 (1 + \lambda V_{DS})$ $(V_{GS} > V_{TN})$ and $(V_{DS} > V_{GS} - V_{TN})$

PMOS

Cutoff $I_D = 0$ $(V_{SG} < |V_{TP}|)$

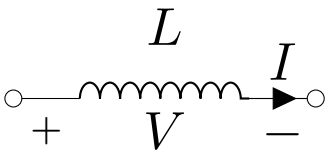
Linear mode

$I_D = \mu_p C_{ox} \frac{W}{L} \left((V_{SG} - |V_{TP}|) V_{SD} - \frac{V_{SD}^2}{2} \right)$ $(V_{SG} > |V_{TP}|)$ and $(V_{SD} < V_{SG} - |V_{TP}|)$

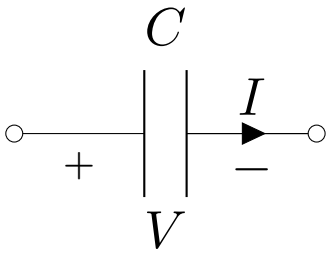
Saturation mode

$I_D = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} (V_{SG} - |V_{TP}|)^2 (1 + \lambda V_{SD})$ $(V_{SG} > |V_{TP}|)$ and $(V_{SD} > V_{SG} - |V_{TP}|)$

Transmission line equations



(a) Inductor



(b) Capacitor

Complex characteristic impedance

$$Z_c = \sqrt{\frac{R+j\omega L}{G+j\omega C}}$$

Characteristic impedance for lossless TL

$$Z_0 = \sqrt{\frac{L}{C}}$$

Inductance voltage-current relation

$$V = L\frac{dI}{dt}$$

Capacitance voltage-current relation

$$I = C\frac{dV}{dt}$$

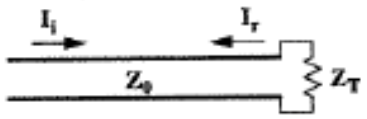
Mutual inductance

$$V_{mn} = L_{mn}\frac{dI_n}{dt} \text{ where } m \neq n$$

Telegrapher's Equation

Reflection Coefficient

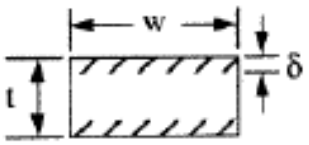
$$k_r = \frac{V_r}{V_i} = \frac{I_r}{I_i} = \frac{Z_T - Z_0}{Z_T + Z_0}$$

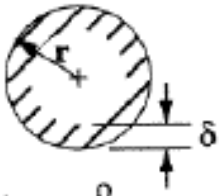


Skin Effect

Skin Depth

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}}$$





Skin Depth Frequency

$$f_s = \frac{\rho}{\pi \mu (t/2)^2} \qquad f_s = \frac{\rho}{\pi \mu r^2}$$

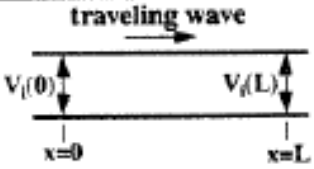
Skin Depth Resistance

$$R(f) = \frac{\sqrt{\pi f \mu \rho}}{2w} = R_{DC}\left(\frac{f}{f_s}\right)^{1/2} \qquad R(f) = \frac{\sqrt{f\mu\rho/\pi}}{2r} = \frac{R_{DC}}{2}\left(\frac{f}{f_s}\right)^{1/2}$$

Attenuation in Lossy Line

Attenuation

$$\frac{V_i(L)}{V_i(0)} = \exp[-(\alpha_R + \alpha_D)L] = \exp\left[-\left(\frac{R}{2Z_0} + \frac{GZ_0}{2}\right)L\right]$$



Conductor Loss

$$\alpha_R(f) = \frac{R_{DC}}{4Z_0}\left(\frac{f}{f_s}\right)^{1/2} \text{ (Round)} \qquad \alpha_R(f) = \frac{R_{DC}}{2Z_0}\left(\frac{f}{f_s}\right)^{1/2} \text{ (Strip)}$$

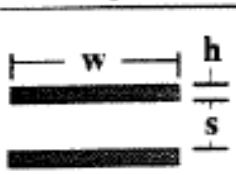
Dielectric Loss (Homogeneous)

$$\alpha_D(f) = \frac{\pi\sqrt{\varepsilon_r}\tan\delta}{c} f$$

Dielectric Loss Tangent

$$\tan\delta = \frac{G}{\omega C} = \frac{\sigma_{Diel}}{\omega \varepsilon_r}$$

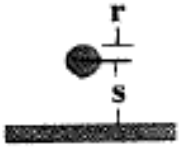
R,C,Z_0 for Various Geometries (Homogeneous Dielectric, $L = \varepsilon\mu/C$)



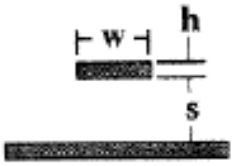
$$R_{DC} = 2\frac{\rho}{wh} \qquad C = \frac{\varepsilon w}{s} \qquad Z_0 = \sqrt{\frac{\mu}{\varepsilon}}\frac{s}{W}$$

$$R_{DC} = \frac{\rho}{\pi r_1^2} + \frac{\rho}{\pi(r_3^2 - r_2^2)} \qquad C = \frac{2\pi\varepsilon}{\log(r_2/r_1)} \qquad Z_0 = \sqrt{\frac{\mu}{\varepsilon}}\frac{\log(r_2/r_1)}{2\pi}$$

$$R_{DC} = \frac{2\rho}{\pi r^2} \qquad C = \frac{\pi\varepsilon}{\log(s/r)} \qquad Z_0 = \sqrt{\frac{\mu}{\varepsilon}}\frac{\log(s/r)}{\pi}$$



$$R_{DC} = \frac{\rho}{\pi r^2} \qquad C = \frac{\pi\varepsilon}{\log(2s/r)} \qquad Z_0 = \sqrt{\frac{\mu}{\varepsilon}}\frac{\log(2s/r)}{\pi}$$



$$R_{DC} = \frac{\rho}{wh} \qquad C = \frac{\varepsilon w}{s} + \frac{2\pi\varepsilon}{\log(s/w)} \qquad Z_0 = \frac{\sqrt{\varepsilon\mu}}{C}$$