TSEK37 Analog CMOS Integrated Circuits

EXAMINATION (TEN1)

Time:	26 August 2015 at 8.00 - 12.00
Place:	TER1
Responsible teacher:	Martin Nielsen-Lönn, ISY, 070-361 52 44 (martin.nielsen.lonn@liu.se)
	Will visit exam location at 8:45 and 10:30.
Number of tasks:	6
Number of pages:	7
Allowed aids:	Calculator, dictionary
Total points:	20
Notes:	Remember to indicate the steps taken when solving problems.
	Please start each new problem at the top of a page!
	Only use one side of each paper!
Exam presentation:	2 September 2015 at 12:00-13:00 in 3D:535, B-building
	Grade Points
	U <8
	3 8 - <12

4

5

12 - <16

16 - 20

(2)

Questions

1) Consider the common-gate amplifier shown in Fig. 1.

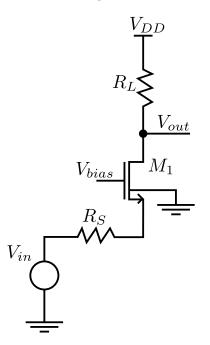


Figure 1: A common-gate amplifier.

- (a) Draw the equivalent small-signal model and derive the expression for the transfer function, DC gain (2) and the two poles. Neglect channel-length modulation and body effect ($\lambda = 0, \gamma = 0$). Consider the parasitic capacitances C_{gs} and C_{gd} in the small-signal model.
- (b) Derive the expression for the input impedance of the amplifier shown in Fig. 1 in terms of g_m , g_{mb} , (1) g_{ds} and R_L . Assume $R_S = 0$ and neglect C_{gs} and C_{gd} . However, channel-length modulation and body effect must be considered ($\lambda \neq 0, \gamma \neq 0$).
- 2) Consider the fully differential amplifier shown in Fig. 2. The amplifier is completely symmetric. Neglect body effect ($\gamma = 0$). However, channel-length modulation must be considered ($\lambda \neq 0$). The parasitic capacitances C_{db} and C_{gs} of the MOSFETs should be considered. Ignore other parasitic capacitances.
 - (a) Draw the small-signal model of the amplifier shown in Fig. 2 and derive the transfer function.
 - (b) Derive the expressions for the DC gain, the two pole frequencies and the unity-gain frequency. (1) Assume that the dominant pole is formed at the output node of the amplifier. Assume $C_L \gg C_{db}$.
 - (c) For $C_L = 10$ pF, let the unity-gain frequency of the amplifier = 1 Mrad/s, the dominant pole (2) frequency = 100 krad/s and the non-dominant pole frequency = 2.5 Mrad/s. Determine the change in phase margin when C_L is reduced to 8 pF. Assume $C_L \gg C_{db}$.

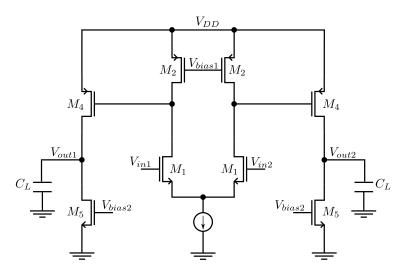


Figure 2: A fully differential amplifier.

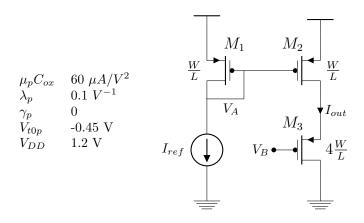


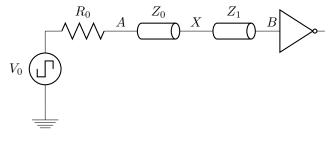
Figure 3: Cascode current mirror.

3) In Fig. 3 a cascode current mirror is shown. The aim here is to copy the reference current I_{ref} to I_{out} . (3) Assume that $V_A = 0.6$ V and all transistors are in saturation. What should V_B then be to make $I_{ref} = I_{out}$?

(3)

4) Figure 4 shows a lossless interconnect circuit. At t = 0 the voltage step V_0 goes high and propagates a pulse through the circuit. Given the values below, calculate the voltage at nodes A and B at t = 7 ns. t_{d,Z_x} is the delay through transmission line Z_x . Assume that the inverters have a infinite (high) input impedance.

 $R_0 = 75 \ \Omega, \ Z_0 = 75 \ \Omega, \ Z_1 = 25 \ \Omega, \ t_{d,Z_0} = 1 \text{ ns and } t_{d,Z_1} = 1.5 \text{ ns.}$





5) The differential inverter shown in Fig. 5 below is used to construct a 6-stage ring oscillator. Assume that the inverter is completely symmetric and all parasitics are neglected except the output capacitance of each stage (i.e. C). Assume that $g_{m1} = g_{m2} = 1.5 \text{ mV/A}$ and $\lambda = \gamma = 0$.

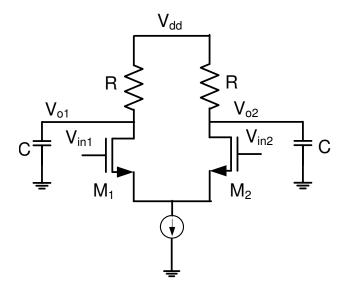


Figure 5: Differential Inverter.

- (a) Draw the circuit of the ring oscillator using this differential inverter. (1/2)
 (b) Calculate the minimum value of the resistance, R required to start the oscillation in this 6-stage circuit. (21/2)
- (c) Explain why a single common-source amplifier stage whose output is connected to its input as shown (1) in the following figure (Fig. 6) cannot function as a ring oscillator.

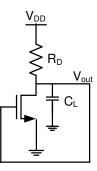
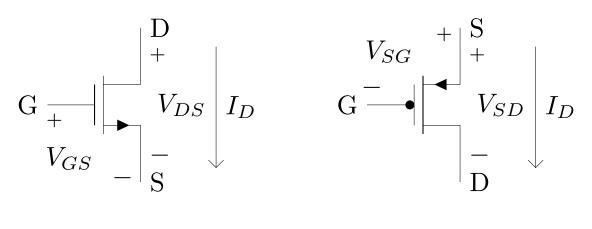


Figure 6: Common Source stage in feedback.

6) An XOR gate is used as a phase detector in a DLL. When the phase difference between the input and the output of the DLL is 225°, draw the input and output waveforms of the phase detector. Also calculate the average output voltage of the phase detector. Assume that the waveforms are ideal square waves with full swing between 0 and 1.2 V.

(2)

Transistor equations



(a) NMOS

(b) PMOS

NMOS

Cutoff

$$(V_{GS} < V_{TN})$$

Linear mode

$$I_D = \mu_n C_{ox} \frac{W}{L} \left((V_{GS} - V_{TN}) V_{DS} - \frac{V_{DS}^2}{2} \right) \quad (V_{GS} > V_{TN}) \text{ and } (V_{DS} < V_{GS} - V_{TN})$$

Saturation mode

 $I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TN})^2 (1 + \lambda V_{DS}) \quad (V_{GS} > V_{TN}) \text{ and } (V_{DS} > V_{GS} - V_{TN})$

PMOS

Cutoff $I_D = 0$ $(V_{SG} < |V_{TP}|)$

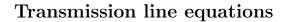
 $I_D = 0$

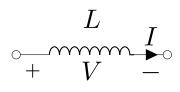
Linear mode

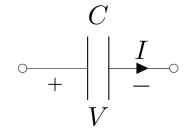
$$I_D = \mu_p C_{ox} \frac{W}{L} \left((V_{SG} - |V_{TP}|) V_{SD} - \frac{V_{SD}^2}{2} \right) \quad (V_{SG} > |V_{TP}|) \text{ and } (V_{SD} < V_{SG} - |V_{TP}|)$$

Saturation mode

$$I_D = \frac{1}{2}\mu_p C_{ox} \frac{W}{L} (V_{SG} - |V_{TP}|)^2 (1 + \lambda V_{SD}) \quad (V_{SG} > |V_{TP}|) \text{ and } (V_{SD} > V_{SG} - |V_{TP}|)$$







(a) Inductor



Complex characteristic impedance

Characteristic impedance for lossless TL

$$Z_c = \sqrt{\frac{R+j\omega L}{G+j\omega C}}$$

$$Z_0 = \sqrt{\frac{L}{C}}$$

Inductance voltage-current relation

Capacitance voltage-current relation

$$V = L \frac{dI}{dt}$$

$$I = C \frac{dV}{dt}$$

Mutual inductance

$$V_{mn} = L_{mn} \frac{dI_n}{dt}$$
 where $m \neq n$

