

EXAMINATION IN
-
TSEK37/TEN1
ANALOG CMOS INTEGRATED
CIRCUITS

Date: 2014-01-18
Time: 8-12
Location: U1
Aids: Calculator, Dictionary
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8 points are required to pass.

Please start each new problem at the top of a page!
Only use one side of each paper!

- 1) Fig. 1 shows a charge pump for a PLL. The switch transistors M1 and M4 have been placed outside the current mirror outputs (M2 and M3) to reduce glitches at the output node.

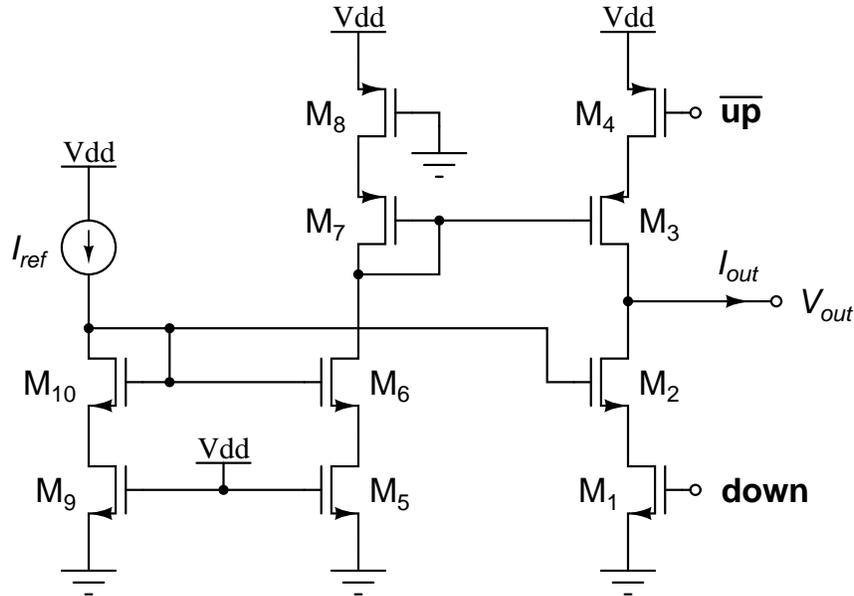


Fig. 1. Charge pump circuit.

All transistor sizes are $10\mu\text{m}$ wide and $0.35\mu\text{m}$ long. Neglect the channel length modulation and the body effect ($\lambda = \gamma = 0$). Assume $I_{\text{ref}} = 10\ \mu\text{A}$, $\mu_n C_{\text{ox}} = 150\ \mu\text{A}/\text{V}^2$, $\mu_p C_{\text{ox}} = 75\ \mu\text{A}/\text{V}^2$, $V_{\text{tn}} = 400\ \text{mV}$, $V_{\text{tp}} = -550\ \text{mV}$ and $V_{\text{dd}} = 3.3\ \text{V}$.

- (a) Considering the timing diagram shown in Fig. 2, calculate the current I_{out} at time t_1 and t_2 , respectively. (2 p)

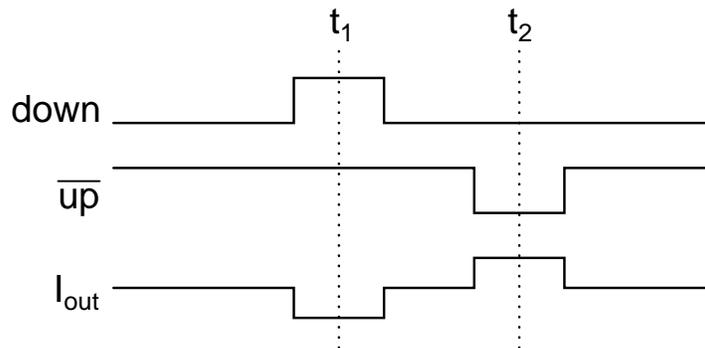


Fig. 2. Timing diagram for the charge pump.

- (b) Calculate the output range of the charge pump. The output range is defined as the voltage range for V_{out} where M2 is saturated when the **down** signal is high and M3 is saturated when the **up** signal is low. (2 p)

- 2) The differential amplifier in Fig. 3 is biased with a current source with finite output resistance R_{SS} (current source is not shown). The transistors in the circuit suffers from transconductance mismatch, i.e. $g_{m1} - g_{m2} = \Delta g_m \neq 0$.

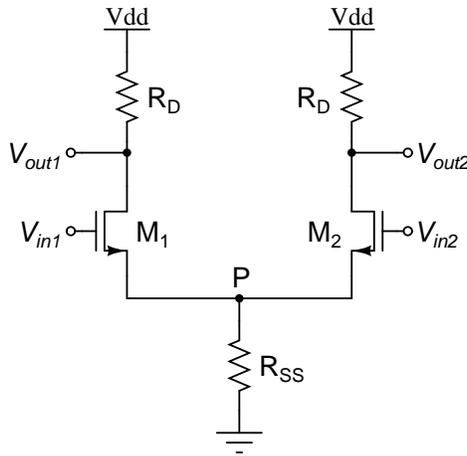


Fig. 3. Differential amplifier circuit biased with non-ideal current source.

Determine an expression for the small-signal common-mode rejection ratio (CMRR) of the circuit. Assume the transistors are operating in the saturation region and that the load resistors are matched. Also neglect the channel-length modulation and body effect. (3 p)

Hint: The common-mode rejection ratio is defined as:

$$CMRR = \left| \frac{A_{DM-DM}}{A_{CM-DM}} \right|$$

where A_{DM-DM} is the gain from a differential input signal to the differential output and A_{CM-DM} is the gain from a common-mode input to the differential output.

- 3) Fig. 4 shows a differential amplifier circuit. The amplifier is completely symmetric. Ignore all parasitic capacitances except for C_X and C_L . Also neglect the channel-length modulation and the body effect ($\lambda = \gamma = 0$).

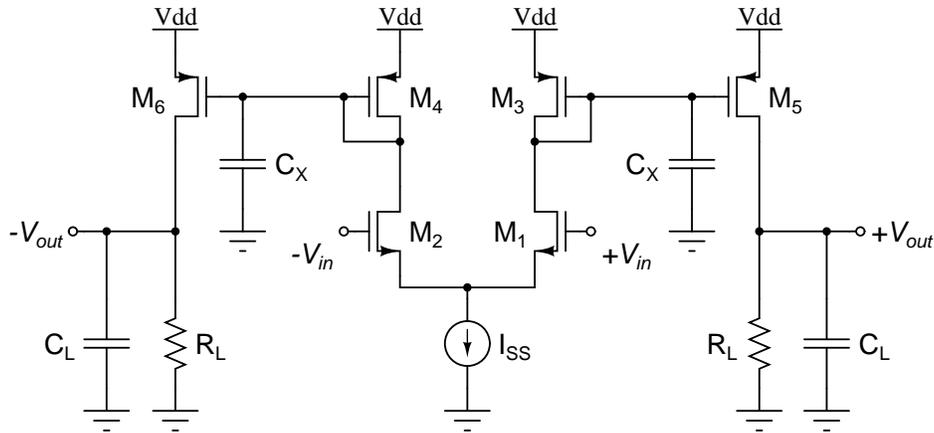


Fig. 4. Differential current mirror amplifier.

- (a) Draw the small-signal model and determine the transfer function of the amplifier. (2 p)
- (b) If $g_{m3}=1.64$ mS, $g_{m5}=4 \cdot g_{m3}$, $R_L=1.5$ k Ω , $C_L=10$ pF, and $C_X=0.5$ pF; calculate the value of g_{m1} to have a unity gain frequency of 2 Grad/s and calculate the phase margin assuming a feedback factor (β) of 1. (2 p)

- 4) A 2-mm RC-wire is divided into m equal-length sections and m identical repeaters are inserted between the sections as shown in Fig. 5. Assume that the delay through an RC wire is $0.38rcd^2$, where d is wire length and r and c are resistance and capacitance per unit length. If $rc = 960$ μ s and the propagation delay of each repeater is 50 ps, calculate the required number of sections to build a non-inverting signal propagation through the line with minimum delay. (3 p)

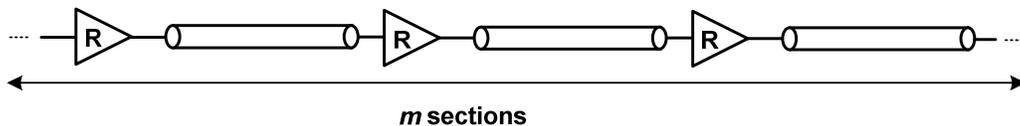


Fig. 5. Inserting repeaters to minimize the delay through the wire.

- 5) A 3-stage ring oscillator is shown in Fig. 6. Assume that the second and third stages are ideal inverters with a switching threshold at $V_{DD}/2$ and their propagation delays are 200 ps and 225 ps, respectively. Furthermore, assume that M_1 and M_4 transistors (in the first stage) are long channel devices and M_2 and M_3 transistors are ideal switches with a switching threshold at $V_{DD}/2$. All of the parasitic capacitances of M_1 and M_4 can be ignored. Calculate the oscillation frequency of the oscillator. (4 p)

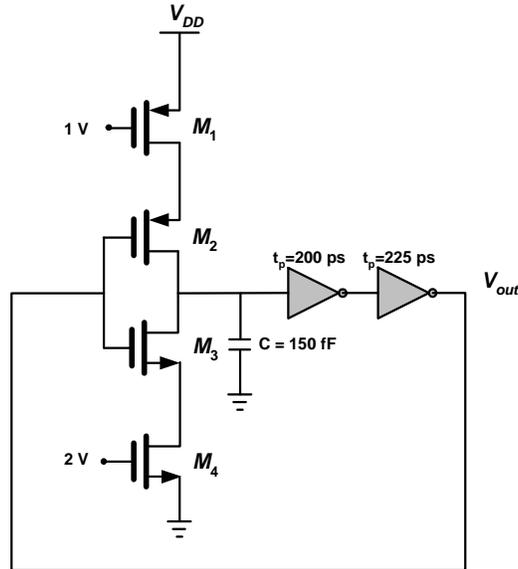


Fig. 6. A three-stage ring oscillator.

Circuit parameters:

$V_{thn} = V_{thp} = 0.5 \text{ V}$	$V_{DD} = 3 \text{ V}$
$\lambda_n = \lambda_p = 0$	$(W/L)_1 = 40$
$C_{ox}\mu_n = 200 \mu\text{A}/\text{V}^2$	$(W/L)_4 = 20$
$C_{ox}\mu_p = 50 \mu\text{A}/\text{V}^2$	$\gamma = 0$

- 6) An XOR gate is utilized as phase detector in a DLL as it is shown in Fig. 7. Draw the input-output characteristic of the phase detector for the interval of $[-2\pi, 2\pi]$ assuming that V_{DD} is 3 V. (2 p)

Hint: Draw the average value of the output voltage ($\overline{V_{out}}$) with respect to $\Delta\phi$, where $\Delta\phi$ is the phase difference between the input signals.

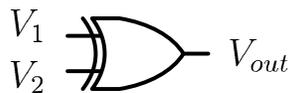
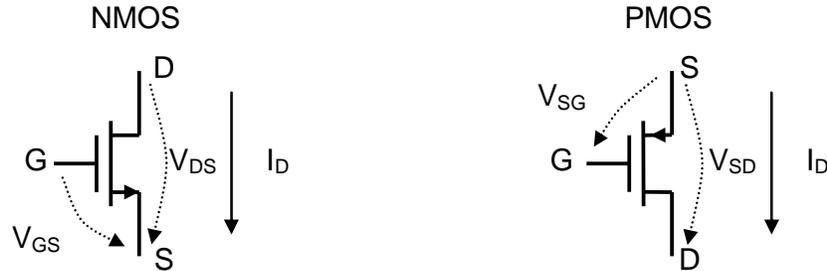


Fig.7. XOR gate as phase detector.

TRANSISTOR EQUATIONS



NMOS

- **Cutoff:** $I_D = 0$ ($V_{GS} < V_{TN}$)
- **Linear mode:**

$$I_D = \mu_n C_{ox} \frac{W}{L} \left((V_{GS} - V_{TN}) V_{DS} - \frac{V_{DS}^2}{2} \right)$$
 ($V_{GS} > V_{TN}$) and ($V_{DS} < V_{GS} - V_{TN}$)
- **Saturation mode:**

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TN})^2 (1 + \lambda V_{DS})$$
 ($V_{GS} > V_{TN}$) and ($V_{DS} > V_{GS} - V_{TN}$)

PMOS

- **Cutoff:** $I_D = 0$ ($V_{GS} < |V_{TP}|$)
- **Linear mode:**

$$I_D = \mu_p C_{ox} \frac{W}{L} \left((V_{SG} - |V_{TP}|) V_{SD} - \frac{V_{SD}^2}{2} \right)$$
 ($V_{GS} > |V_{TP}|$) and ($V_{SD} < V_{SG} - |V_{TP}|$)
- **Saturation mode:**

$$I_D = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} (V_{SG} - |V_{TP}|)^2 (1 + \lambda V_{SD})$$
 ($V_{GS} > |V_{TP}|$) and ($V_{SD} > V_{SG} - |V_{TP}|$)

TRANSMISSION LINE EQUATIONS

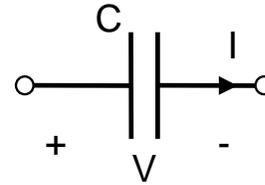
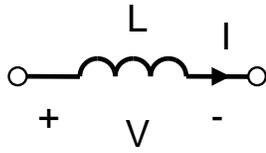
- Complex characteristic impedance

$$Z_c = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$
- Inductance voltage-current relation:

$$V = L \frac{dI}{dt}$$
- Characteristic impedance for lossless TL:

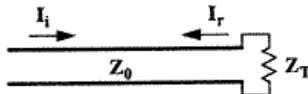
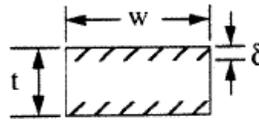
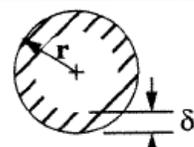
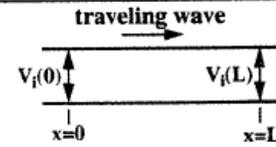
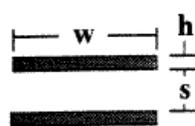
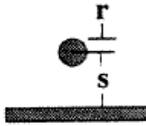
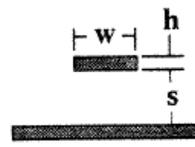
$$Z_0 = \sqrt{\frac{L}{C}}$$
- Capacitance voltage-current relation:

$$I = C \frac{dV}{dt}$$



- Mutual inductance:

$$V_{mn} = L_{mn} \frac{dI_n}{dt} \text{ where } m \neq n$$

Telegrapher's Equation				
Reflection Coefficient	$k_r = \frac{V_r}{V_i} = \frac{I_r}{I_i} = \frac{Z_T - Z_0}{Z_T + Z_0}$ 			
Skin Effect	 			
Skin Depth	$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}}$			
Skin Depth Frequency	$f_s = \frac{\rho}{\pi \mu (t/2)^2} \quad f_s = \frac{\rho}{\pi \mu r^2}$			
Skin Depth Resistance	$R(f) = \frac{\sqrt{\pi f \mu \rho}}{2w} = R_{DC} \left(\frac{f}{f_s}\right)^{1/2} \quad R(f) = \frac{\sqrt{f \mu \rho / \pi}}{2r} = \frac{R_{DC}}{2} \left(\frac{f}{f_s}\right)^{1/2}$			
Attenuation in Lossy Line				
Attenuation	$\frac{V_i(L)}{V_i(0)} = \exp[-(\alpha_R + \alpha_D)L] = \exp\left[-\left(\frac{R}{2Z_0} + \frac{GZ_0}{2}\right)L\right]$ 			
Conductor Loss	$\alpha_R(f) = \frac{R_{DC}}{4Z_0} \left(\frac{f}{f_s}\right)^{1/2} \text{ (Round)} \quad \alpha_R(f) = \frac{R_{DC}}{2Z_0} \left(\frac{f}{f_s}\right)^{1/2} \text{ (Strip)}$			
Dielectric Loss (Homogeneous)	$\alpha_D(f) = \frac{\pi \sqrt{\epsilon_r} \tan \delta}{c} f \quad \text{Dielectric Loss Tangent } \tan \delta = \frac{G}{\omega C} = \frac{\sigma_{Diel}}{\omega \epsilon_r}$			
R,C,Z0 for Various Geometries (Homogeneous Dielectric, L = εμ/C)				
				
$R_{DC} = 2 \frac{\rho}{wh}$	$R_{DC} = \frac{\rho}{\pi r_1^2} + \frac{\rho}{\pi (r_2^2 - r_1^2)}$	$R_{DC} = \frac{2\rho}{\pi r^2}$	$R_{DC} = \frac{\rho}{\pi r^2}$	$R_{DC} = \frac{\rho}{wh}$
$C = \frac{\epsilon w}{s}$	$C = \frac{2\pi \epsilon}{\log(r_2/r_1)}$	$C = \frac{\pi \epsilon}{\log(s/r)}$	$C = \frac{\pi \epsilon}{\log(2s/r)}$	$C = \frac{\epsilon w}{s} + \frac{2\pi \epsilon}{\log(s/w)}$
$Z_0 = \sqrt{\frac{\mu s}{\epsilon W}}$	$Z_0 = \sqrt{\frac{\mu \log(r_2/r_1)}{\epsilon 2\pi}}$	$Z_0 = \sqrt{\frac{\mu \log(s/r)}{\epsilon \pi}}$	$Z_0 = \sqrt{\frac{\mu \log(2s/r)}{\epsilon \pi}}$	$Z_0 = \frac{\sqrt{\epsilon \mu}}{C}$