LINKÖPING UNIVERSITY
Behzad Mesgarzadeh
Daniel Svärd
Electronic Devices, Department of Electrical Engineering

ANSWERS
-
TSEK37 ANALOG CMOS INTEGRATED CIRCUITS

Date:	2014-01-18
Time:	8-12
Location:	U1
Aids:	Calculator, Dictionary
Teachers:	Behzad Mesgarzadeh (5719)
	Daniel Svärd (8946)

8 points are required to pass.

Please start each new problem at the top of a page!
Only use one side of each paper!

1)

(a)

At time $\mathbf{t_1}$, transistors M1, M5 and M9 have the same bias point. The drain-source voltage drop is therefore equal for all three transistors. The source-gate voltage for transistor M2, M6 and M10 are therefore identical. With ($\lambda = \gamma = 0$), the current through the transistors M2, M6 and M10 will therefore be identical. I_D for M10 = I_{ref} => I_D for M2 = I_D for M5 = I_{ref}. In a similar manner, transistor M4 and M8 will have identical bias points at time $\mathbf{t_2}$, resulting in identical gate-source voltages for transistor M3 and M7 giving that I_D for M3 = I_D for M7 = I_D for M6 = I_{ref}.

So I_{out} at time $t_1 = -I_{ref} = -10$ µA and I_{out} for time $t_2 = I_{ref} = 10$ µA.

(b)

When the down signal is high, transistor M1 will be in the linear region. From (a) we know that the current I_D will be 10 µA.

Transistor equation for a NMOS transitor in the linear region:

$$I_D = \mu_n C_{ox}\frac{W}{L}\left((V_{GS}-V_{TN})V_{DS}-\frac{V_{DS}^2}{2}\right) => V_{DS} = (V_{GS}-V_{TN}) \pm \sqrt{(V_{GS}-V_{TN})^2 - \frac{2I_D}{\mu_n C_{ox}\frac{W}{L}}} =>$$

$$V_{DS} = \begin{cases} 0.83mV \\ (5.799V) \end{cases}$$

Transistor M10 is always in saturation. V_{GS} is then given from:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TN})^2(1+\lambda V_{DS}) => V_{GS} = \sqrt{\frac{I_D}{(1+\lambda V_{DS})}\frac{2}{\mu_n C_{ox}\frac{W}{L}}} + V_{TN} => V_{GS} = 0.4683V$$

which is also the V_{GS} for transistor M2.

Transistor M2 is in saturation as long as ($V_{GS} > V_{TN}$) and ($V_{DS} > V_{GS} - V_{TN}$)
$V_{DS} = V_{GS} - V_{TN} = 0.4683V - 0.4\ V = 68.3mV$
The minimum output voltage is then $V_{DSM1} + V_{DSM2} = 0.83mV + 68.3\ mV = 69.1mV$

The same calculation as for transistor M1 gives for transistor M4:

$$I_D = \mu_p C_{ox}\frac{W}{L}\left((V_{SG}-|V_{TP}|)V_{SD}-\frac{V_{SD}^2}{2}\right) => V_{SD} = (V_{SG}-|V_{TP}|) \pm \sqrt{(V_{SG}-|V_{TP}|)^2 - \frac{2I_D}{\mu_p C_{ox}\frac{W}{L}}}$$

$$=> V_{SD} = \begin{cases} 1.697mV \\ (5.498V) \end{cases}$$

The same calculation as for transistor M10 gives for M7

$$I_D = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}\left(V_{SG}-|V_{TP}|\right)^2\left(1+\lambda V_{SD}\right) => V_{SG} = \sqrt{\frac{I_D}{\left(1+\lambda V_{SD}\right)}\frac{2}{\mu_p C_{ox}\frac{W}{L}}}+|V_{TP}| =>$$

$V_{SG} = 0.6466V$ which is also the V_{SG} for transistor M3.

Transistor M3 is in saturation as long as ($V_{GS} > |V_{TP}|$) and ($V_{SD} < V_{SG} - |V_{TP}|$)
$V_{SD} = V_{SG} - |V_{TP}| = 0.6466V – 0.55\ V = 96.6mV$
The maximum output voltage is then $V_{dd} - V_{SDM4} - V_{DSM3} = 3.3 – 1.697mV – 96.6\ mV = 3.202V$

The output range of the charge pump is thus $69.1mV < V_{out} < 3.202\ V$.

2)

Start by deriving an expression for each output voltage, V_{out1} and V_{out2}, as a function of the input voltages V_{in1} and V_{in2}.

$$V_{out1} = -g_{m1}R_D\left(V_{in1}-V_P\right)$$
$$V_{out2} = -g_{m2}R_D\left(V_{in2}-V_P\right)$$

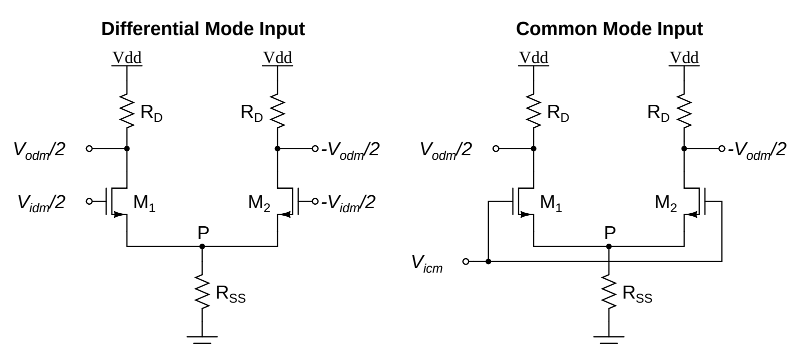
The voltage at node P is equal to the voltage drop over R_{SS} generated by the total drain current of the two transistors.

$$V_P = \left(I_{D1}+I_{D2}\right)R_{SS} = g_{m1}\left(V_{in1}-V_P\right)R_{SS} + g_{m2}\left(V_{in2}-V_P\right)R_{SS} \Rightarrow$$
$$V_P = \frac{g_{m1}V_{in1}+g_{m2}V_{in2}}{\left(g_{m1}+g_{m2}\right)R_{SS}+1}R_{SS}$$

The voltages at outputs, V_{out1} and V_{out2}, can then be found by substituting V_P for the expression above and simplifying:

$$V_{out1} = -g_{m1}R_D\left(V_{in1}-V_P\right) = -\frac{g_{m1}R_D}{\left(g_{m1}+g_{m2}\right)R_{SS}+1}\left(V_{in1}+\left(V_{in1}-V_{in2}\right)g_{m2}R_{SS}\right)$$
$$V_{out2} = -g_{m2}R_D\left(V_{in2}-V_P\right) = -\frac{g_{m2}R_D}{\left(g_{m1}+g_{m2}\right)R_{SS}+1}\left(V_{in2}+\left(V_{in2}-V_{in1}\right)g_{m1}R_{SS}\right)$$

Now we need to find the gain for the two different input configurations shown below:



Differential mode: $A_{DM-DM} = \frac{V_{odm}}{V_{idm}} = \frac{V_{out1} - V_{out2}}{V_{in1} - V_{in2}}$

We insert $V_{in1}=V_{idm}/2$ and $V_{in2}=-V_{idm}/2$ into the expressions for V_{out1} and V_{out2} above to get:

$$V_{out1} = \frac{V_{odm}}{2} = -\frac{g_{m1}R_D}{(g_{m1}+g_{m2})R_{SS}+1}(1+2g_{m2}R_{SS})\frac{V_{idm}}{2}$$

$$V_{out2} = -\frac{V_{odm}}{2} = \frac{g_{m2}R_D}{(g_{m1}+g_{m2})R_{SS}+1}(1+2g_{m1}R_{SS})\frac{V_{idm}}{2}$$

Now we find the differential gain as:

$$A_{DM-DM} = \frac{V_{out1}-V_{out2}}{V_{idm}} = -\frac{R_D}{2}\frac{g_{m1}+g_{m2}+4g_{m1}g_{m2}R_{SS}}{(g_{m1}+g_{m2})R_{SS}+1}$$

Common mode: $A_{CM-DM} = \frac{V_{odm}}{V_{icm}} = \frac{V_{out1} - V_{out2}}{V_{icm}}$

We insert $V_{in1}=V_{in2}=V_{icm}$ into the expressions for V_{out1} and V_{out2} above to get:

$$V_{out1} = -\frac{g_{m1}R_D}{(g_{m1}+g_{m2})R_{SS}+1}V_{icm}$$

$$V_{out2} = -\frac{g_{m2}R_D}{(g_{m1}+g_{m2})R_{SS}+1}V_{icm}$$

Now we find the common-mode gain as:

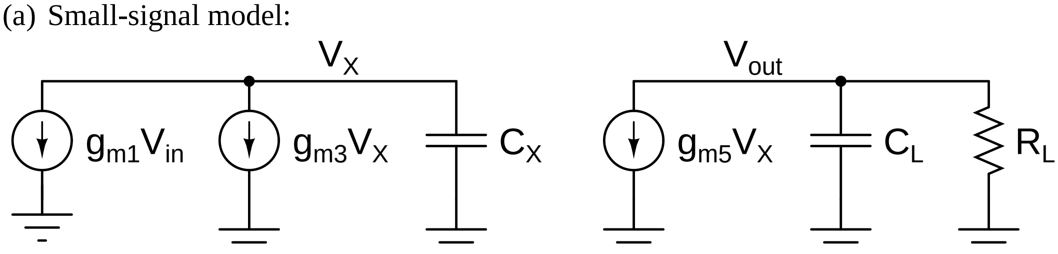
$$A_{CM-DM} = \frac{V_{out1}-V_{out2}}{V_{icm}} = -\frac{(g_{m1}-g_{m2})R_D}{(g_{m1}+g_{m2})R_{SS}+1} = -\frac{\Delta g_m R_D}{(g_{m1}+g_{m2})R_{SS}+1}$$

So the common-mode rejection ratio is:

$$CMRR = \left|\frac{A_{DM-DM}}{A_{CM-DM}}\right| = \frac{g_{m1}+g_{m2}+4g_{m1}g_{m2}R_{SS}}{2\Delta g_m}$$

3)

(a) Small-signal model:



Write the nodal equations for the circuit:

KCL @ V_X: $$g_{m1}V_{in} + g_{m3}V_X + sC_XV_X = 0 \Rightarrow V_X = -\frac{g_{m1}}{g_{m3}+sC_X}V_{in}$$

KCL @ V_{out}: $$g_{m5}V_X + sC_L V_{out} + \frac{V_{out}}{R_L} = 0 \Rightarrow V_{out} = -\frac{g_{m5}R_L}{1+sC_L R_L}V_X$$

The transfer function is then found to be:

$$H(s) = \frac{V_{out}}{V_{in}}(s) = \frac{g_{m1}g_{m5}R_L}{g_{m3}} \cdot \frac{1}{1+sC_L R_L} \cdot \frac{1}{1+s\frac{C_X}{g_{m3}}}$$

(b) We rewrite the transfer function in terms of the DC gain, A_0, and the two poles ω_{p1} and ω_{p2}.

$$H(s) = A_0 \cdot \frac{1}{1+\frac{s}{\omega_{p1}}} \cdot \frac{1}{1+\frac{s}{\omega_{p2}}}$$

where $A_0 = \frac{g_{m1}g_{m5}R_L}{g_{m3}} = 6000 g_{m1}$ $\quad \omega_{p1} = \frac{1}{C_L R_L} = \frac{2}{30}$ Grad/s $\quad \omega_{p2} = \frac{g_{m3}}{C_X} = 3.28$ Grad/s

The unity gain frequency, ω_u = 2 Grad/s, occurs when $|H(j\omega_u)| = 1$.

$$|H(j\omega_u)| = A_0 \cdot \frac{1}{\sqrt{1+\left(\frac{\omega_u}{\omega_{p1}}\right)^2}} \cdot \frac{1}{\sqrt{1+\left(\frac{\omega_u}{\omega_{p2}}\right)^2}} = 1$$

$$\Rightarrow A_0 = \sqrt{1+\left(\frac{2\times 30}{2}\right)^2} \cdot \sqrt{1+\left(\frac{2}{3.28}\right)^2} \approx 35.1 \Rightarrow g_{m1} = 5.85\,\text{mS}$$

The phase margin is defined as $PM = 180° + \angle\beta H(j\omega_u) = 180° + \angle H(j\omega_u)$ if β=1.

$$\angle H(j\omega_u) = -\arctan\left(\frac{\omega_u}{\omega_{p1}}\right) - \arctan\left(\frac{\omega_u}{\omega_{p2}}\right) = -\arctan\left(\frac{2\times 30}{2}\right) - \arctan\left(\frac{2}{3.28}\right) \approx -119.5°$$

So the phase margin is

$$PM = 180° - 119.5° = 60.5°$$

4)

The total delay $D = mt_p + m\left[0.38(\frac{d}{m})^2 rc\right] = mt_p + 0.38\frac{d^2}{m}rc$

For optimum delay we should have $\frac{dD}{dm} = t_p - 0.38\frac{d^2}{m^2}rc = 0$

$$m_{opt} = \sqrt{\frac{0.38rcd^2}{t_p}}$$

Replacing the values for *rc*, *d* and t_p results in:

$$m_{opt} = \sqrt{\frac{0.38 \times 960 \times 10^{-6} (2 \times 10^{-3})^2}{50 \times 10^{-12}}} = 5.4$$

Since the line is non-inverting then we choose $m = 6$.

5)

a) Initially we assume that V_{out}=0 and there is no charge on C. M_3 is off and M_2 is on and M_1 charges the capacitor. Then V_{DS1}=3 and V_{GS1}-|V_t|=1.5 and M_1 is in saturation:

$$I_1 = \frac{1}{2} \times 50 \times 40 \times 10^{-6} \times (2 - 0.5)^2 = 2.25 \text{ mA}$$

M_1 will be in saturation region until V_{DS1}=V_{GS1}-|V_t|=1.5 V or the voltage on capacitor is 1.5 V which is the switching threshold for the coming stage. To get this point:

$$\Delta t = \frac{C \cdot \Delta V}{I_1} = \frac{150 \times 10^{-15} \times 1.5}{2.25 \times 10^{-3}} = 100 \text{ ps}$$

From this point on, after 200+225=425 ps V_{out} goes 1. Now we should calculate the time in which the output of the first stage reaches to V_{DD}. When M_1 enters the linear region, to have a rough estimation about the charging time we can assume that the capacitor is charged with a constant current which is the average of the currents in the beginning and end of the transition. Then:

$$I_1(V_c = 1.5) = 50 \times 40 \times 10^{-6} \times (1.5^2 - \frac{1.5^2}{2}) = 2.25 \text{ mA}$$

$$I_1(V_c = 3) = 50 \times 40 \times 10^{-6} \times (1.5 \times 0 - \frac{0^2}{2}) = 0 \text{ mA}$$

$$\Delta t = \frac{C \cdot \Delta V}{I_{1avg}} = \frac{150 \times 10^{-15} \times 1.5}{1.125 \times 10^{-3}} = 200 \text{ ps}$$

Since 200 ps is less than the total propagation delay in the second and third stages (425 ps) then the voltage at the output of the first stage reaches V_{DD} before the next transition.

When V_{out} goes high, M_3 is on and M_2 is off and C is discharged by M_4. To reach V_{DD}/2 which is the switching point for the coming stage:

$$I_4 = \frac{1}{2} \times 200 \times 20 \times 10^{-6} \times (2 - 0.5)^2 = 4.5 \text{ mA}$$

M_4 will be in saturation region until V_{DS4}=V_{GS4}-V_t=1.5 V or the voltage on capacitor is 1.5 V which is the switching threshold for the coming stage. To get this point:

$$\Delta t = \frac{C \cdot \Delta V}{I_4} = \frac{150 \times 10^{-15} \times 1.5}{4.5 \times 10^{-3}} = 50\,\text{ps}$$

From this point on, after 425 ps V_{out} goes low. Using a similar method we can be sure that the capacitor is completely discharged before the next transition. Then V_{out} is 425+50=475 ps at high and 425+100= 525 ps at low. The period is 475+525=1000 ps=1 ns and the oscillation frequency is 1 GHz.

6)