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ANSWERS
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TSEK37 ANALOG CMOS INTEGRATED CIRCUITS

Date:	2012-04-13
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Location:	TER2
Aids:	Calculator, Dictionary
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8 points are required to pass.

Please start each new problem at the top of a page!
Only use one side of each paper!

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1)

(a) For M_1 to be in saturation we have:

$$V_{GS1} - V_{TH1} \le V_{DS1} \Rightarrow V_{GS1} - V_{TH1} \le V_b - V_{GS2}$$

For M_2 to be in saturation we have:

$$V_{GS2} - V_{TH2} \le V_{DS2} \Rightarrow V_b - V_{TH2} \le V_{GS1}$$

So combining these two expressions we get the following bounds on V_b:

$$V_{GS2} + (V_{GS1} - V_{TH1}) \le V_b \le V_{GS1} + V_{TH2}$$

A solution to this relation only exists if

$$V_{GS2} + (V_{GS1} - V_{TH1}) \le V_{GS1} + V_{TH2} \Rightarrow V_{GS2} - V_{TH2} \le V_{TH1}$$

This means that we must size M_2 such that its overdrive voltage is less than one threshold voltage.

(b) For M_4 to be in saturation we have:

$$V_{GS4} - V_{TH4} \le V_{DS4} \Rightarrow V_b - V_{TH4} \le V_P$$

So for the lowest V_P and the lowest V_b we have:

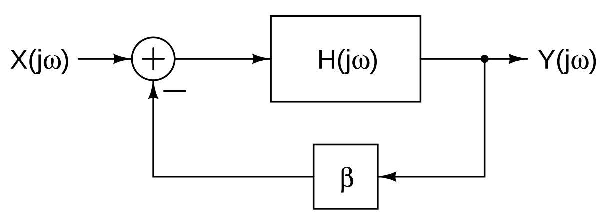
$$V_P = V_b - V_{TH4} = V_{GS2} + V_{GS1} - V_{TH1} - V_{TH4}$$

If $M_3 = M_1$ and $V_{GS4} = V_{GS2}$, then:

$$V_P = (V_{GS3} - V_{TH3}) + (V_{GS4} - V_{TH4})$$

So the minimum voltage headroom consumed by the current mirror is two overdrive voltages.

2) The figure below shows a general feedback system.



The closed-loop transfer function of this system can be found to be

$$\frac{Y(j\omega)}{X(j\omega)} = \frac{H(j\omega)}{1+\beta H(j\omega)}.$$

From the problem description we have that β=1/4 and

$$H(j\omega) = \frac{A_0}{\left(1+j\dfrac{\omega}{\omega_{p1}}\right)\left(1+j\dfrac{\omega}{\omega_{p2}}\right)},$$

where $\omega_{p1} = 2\pi\times 1$ Mrad/s and $\omega_{p2} = 2\pi\times 450$ Mrad/s.

To find the phase margin we need to look at the loop transfer function βH(jω). To make calculations easier we first rewrite the loop transfer function on complex exponential form:

$$\beta H(j\omega) = \frac{\beta A_0}{\sqrt{1+\left(\dfrac{\omega}{\omega_{p1}}\right)^2}\exp\left(j\arctan\dfrac{\omega}{\omega_{p1}}\right)\sqrt{1+\left(\dfrac{\omega}{\omega_{p2}}\right)^2}\exp\left(j\arctan\dfrac{\omega}{\omega_{p2}}\right)} =$$

$$= \frac{\beta A_0}{\sqrt{1+\left(\dfrac{\omega}{\omega_{p1}}\right)^2}\sqrt{1+\left(\dfrac{\omega}{\omega_{p2}}\right)^2}}\times\exp\left[-j\left(\arctan\frac{\omega}{\omega_{p1}}+\arctan\frac{\omega}{\omega_{p2}}\right)\right]$$

We now look at the phase response to find the frequency (ω_u) at which the phase has shifted 60° – 180° = –120°. Here we use the identity from the hint.

$$-\arctan\frac{\omega_u}{\omega_{p1}} - \arctan\frac{\omega_u}{\omega_{p2}} = -120° \Leftrightarrow -\arctan\left(\frac{\omega_u(\omega_{p1}+\omega_{p2})}{\omega_{p1}\omega_{p2}-\omega_u^2}\right) = -120°$$

$$\Rightarrow \frac{\omega_u(\omega_{p1}+\omega_{p2})}{\omega_{p1}\omega_{p2}-\omega_u^2} = -\sqrt{3}$$

Solving this equation for ω_u and plugging in the values for the poles gives:

$$\omega_u = \frac{(\omega_{p1}+\omega_{p2}) \pm \sqrt{(\omega_{p1}+\omega_{p2})^2 + 12\omega_{p1}\omega_{p2}}}{2\sqrt{3}} = \begin{cases} 1646834563 \text{ rad/s} \\ -10787536.48 \text{ rad/s} \end{cases}$$

Since the second solution is negative, we use the first solution for the frequency of -120 degrees phase shift. Now we can look at the magnitude of the loop transfer function to find the value of A_0 that yields a unity gain frequency of ω_u.

$$\left|\beta H(j\omega)\right| = \frac{\beta A_0}{\sqrt{1+\left(\frac{\omega_u}{\omega_{p1}}\right)^2}\sqrt{1+\left(\frac{\omega_u}{\omega_{p2}}\right)^2}} = 1$$

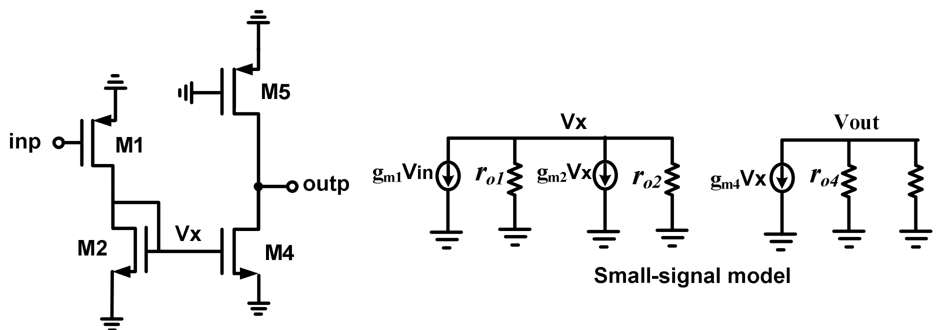
Solving this equation for A_0 and plugging in the values for β, ω_u, ω_{p1} and ω_{p2} gives:

$$A_0 = \frac{1}{\beta}\sqrt{1+\left(\frac{\omega_u}{\omega_{p1}}\right)^2}\sqrt{1+\left(\frac{\omega_u}{\omega_{p2}}\right)^2} \approx 1213$$

The DC gain of the amplifier must therefore be 1213 V/V or 61.7 dB.

3)

(a) The half-circuit and corresponding small-signal model is shown below.



Writing two KCLs at nodes V_X and Vout and noting that $g_{ds}=ro^{-1}$ we get:
at node V_X:

$$g_{m1}Vin + (g_{ds1} + g_{m2} + g_{ds2})V_x = 0 \Rightarrow \frac{V_x}{Vin} = \frac{-g_{m1}}{g_{ds1} + g_{ds2} + g_{m2}} \qquad (1)$$

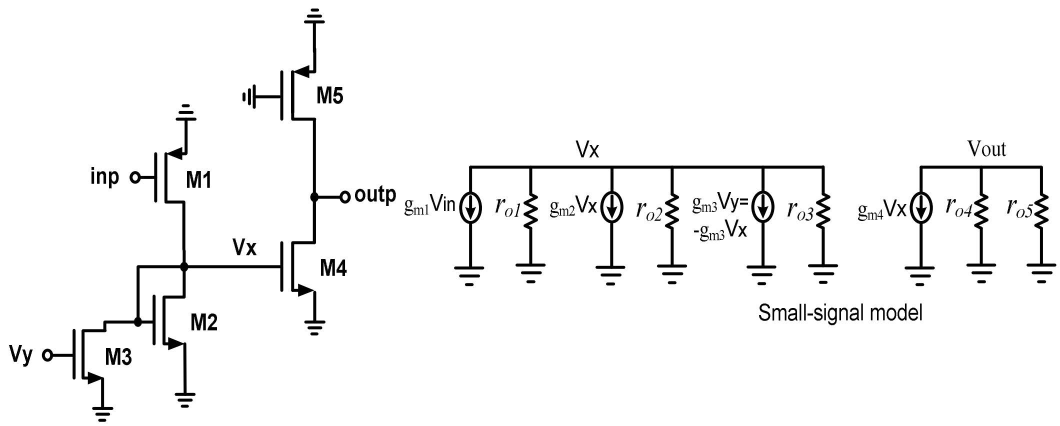
at node V_{out}:

$$g_{m4}Vx + (g_{ds4} + g_{ds5})Vout = 0 \qquad (2)$$

Combining (1) and (2) we obtain

$$\Rightarrow \quad DCgain = \frac{Vout}{Vin} = \frac{g_{m1}}{g_{ds1} + g_{ds2} + g_{m2}} \cdot \frac{g_{m4}}{g_{ds4} + g_{ds5}} \qquad (3)$$

(b) The half-circuit and corresponding small-signal model is shown below.



Due to transistor M_3, two more terms appers in equation (1) as given

$$g_{m1}Vin + (g_{ds1} + g_{m2} + g_{ds2} + g_{ds3} - g_{m3})V_x = 0 \quad \Rightarrow$$

$$\frac{V_x}{Vin} = \frac{-g_{m1}}{g_{ds1} + g_{ds2} + g_{m2} + g_{ds3} - g_{m3}} \tag{4}$$

at node V_{out}: similar to part (b)

$$g_{m4}Vx + (g_{ds4} + g_{ds5})Vout = 0 \tag{5}$$

Combining (4) and (5) we obtain

$$\Rightarrow \quad DCgain = \frac{Vout}{Vin} = \frac{g_{m1}}{g_{ds1} + g_{ds2} + g_{m2} + g_{ds3} - g_{m3}} \cdot \frac{g_{m4}}{g_{ds4} + g_{ds5}} \tag{6}$$

As can be seen from (6), the transistor M_3 can be sized such that the transconductance g_{m3} to be 70-80% of the term $g_{ds1} + g_{ds2} + g_{m2} + g_{ds3}$. This method enhances the DC gain.

(c) The dominate pole due to load capacitance C_L:

$$P_1 = \frac{1}{2\pi.(r_{o4} // r_{o5}).C_L} \qquad (7)$$

The 2nd pole due to parasitic capacitance C_C at the gate of M_2, M_3, and M_4, mainly because of the gate-source capacitance of the devices.

$$P_2 = \frac{1}{2\pi.(1/g_{m2}).C_C} = \frac{g_{m2}}{2\pi.C_C} \qquad (8)$$

4)

From A:

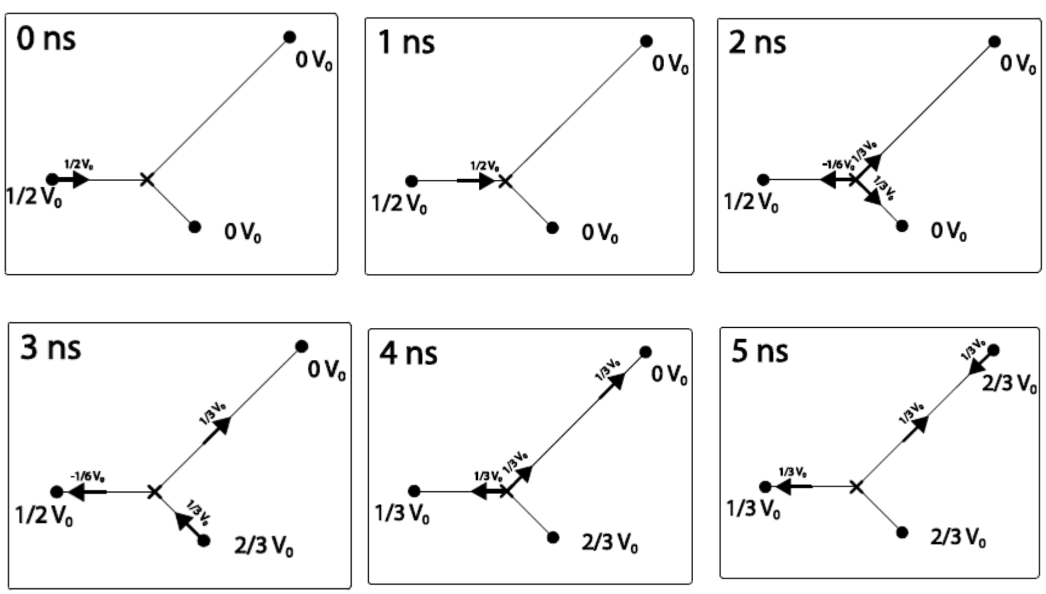
$$\Gamma_{r,A} = \frac{Z_1 // Z_2 - Z_0}{Z_1 // Z_2 + Z_0} = -1/3 \;, \qquad T_A = 1 + \frac{Z_1 // Z_2 - Z_0}{Z_1 // Z_2 + Z_0} = +2/3$$

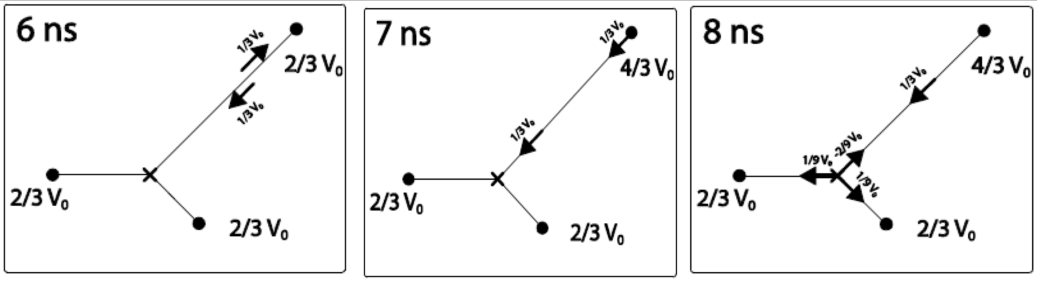
From B:

$$\Gamma_{r,B} = \frac{Z_0 // Z_2 - Z_1}{Z_0 // Z_2 + Z_1} = -2/3 \;, \qquad T_B = 1 + \frac{Z_0 // Z_2 - Z_1}{Z_0 // Z_2 + Z_1} = +1/3$$

From C:

$$\Gamma_{r,C} = \frac{Z_0 // Z_1 - Z_2}{Z_0 // Z_1 + Z_2} = 0 \;, \qquad T_C = 1 + \frac{Z_0 // Z_1 - Z_2}{Z_0 // Z_1 + Z_2} = 1$$





at 7.5ns: $V_A = 2/3V_0$, $V_B = 4/3V_0$ and $V_C = 2/3V_0$

5)

See example 14.17 in the text book and also lecture notes. Spectrum consists of a carrier tone at ω_0 and two tones at $\omega_0 - \omega_m$ and $\omega_0 + \omega_m$.

6)

The PLL expereinces a frequency step of 0.5 MHz and the final value of the PLL output frequency change should be within 100 Hz from 0.5 MHz. For the worst-case, we can put the sine function equal to 1. Then:

$$\omega_{out}(t) = \left\{1 - \frac{1}{\sqrt{1-\zeta^2}} \cdot e^{-\zeta\omega_n t} \sin\left(\omega_n \sqrt{1-\zeta^2} + \theta\right)\right\} \Delta\omega u(t)$$

$$\frac{1}{\sqrt{1-\zeta^2}} \approx 1 \Rightarrow$$

$$0.5 \times 10^6 - 100 = \left(1 - e^{-\zeta\omega_n t_s}\right) \times 0.5 \times 10^6 \Rightarrow e^{-\zeta\omega_n t_s} = \frac{100}{0.5 \times 10^6}$$

$$e^{-\zeta\omega_n t_s} = 2 \times 10^{-4} \Rightarrow \zeta\omega_n t_s = 8.5 \Rightarrow t_s = \frac{17}{\omega_{LPF}} = 94.6\ \mu s$$