VLSI Chip Design Project TSEK06

Project Description and Requirement Specification

Project: DLL-Based Frequency Multiplier

Project number: 3

Project Group:

Name	Project members	Telephone	E-mail
	Project leader and designer		
	Designer		
	Designer		
	Designer		
	Designer		
	Designer		
	Designer		
	Designer		

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1 Background

This document describes the design requirement specification of a DLL-based frequency multiplier. Typically PLLs are utilized for frequency synthesis purpose. Due to the possible stability issues, the PLL design is very challenging and time-consuming task. On the other hand, DLLs utilize a first-order feedback loop enjoying ensured stability. Since in DLLs only a delayed version of the reference clock is generated, frequency multiplication requires extra circuitry. In this project the objective is to design and implement a fully integrated DLL-based frequency multiplier.

1.1 Project goal

The project goal is to design an integrated clock frequency multiplier with >1 GHz output frequency based on a Delay-Locked-Loop (DLL) clock phase generator in a standard 0.35µm CMOS technology. The exact frequency multiplication factor will be decided during the project group meeting with the supervisor. Students participating in this project as project members and project leaders, should learn the different steps of the IC design flow. That includes the given system architecture analysis, simulation, layout implementation and verification. The design is required to be fully completed, evaluated by post-layout simulations, including all I/O pads.

1.2 Milestones and deadline

1	**Project selection**	**Jan 23**
2	Pre-study, project planning, and discussion with supervisor	Jan 23-30
3	High-level modeling design and simulation result (report)	Feb 11
4	Gate/transistor level design and simulations result (report)	Mar 18
5	Layout, DRC, parasitic extraction, LVS, post-layout simulations, modification and chip evaluations.	May 6
6	**DEADLINE** Delivery of the completed chip.	**May 16**
7	**DEADLINE**, Final report, and oral presentation	**May 23**

1.3 Parties

The following parties are involved in this project:

1- Customer and project supervisor: Atila Alvandpour

Tasks:

- Formulates the project requirements
- Provides technical support
- Reviews the project documents.

2- Project leader: One of the members in the design team.

Tasks:

- Responsible for organization of the team and the project planning.
- Divides the design and documentation work in an efficient way
- Organizes the team meetings as well as the meetings between the team and supervisor.
- Keeps the supervisor informed about the progress of the project (at least one e-mail or meeting per week)

3- Project design members (including the project leader)

- Are equally responsible for project planning and design.
- Participate actively in all the meetings
- Support the team and the project leader
- Keep the team and project leader informed about the progress of their tasks.

2 Project description

2.1 System description

The complete system to be built should include the frequency multiplier, on-chip evaluation circuits, and I/O circuitry. Figure 1 shows system level block diagrams of the DLL based clock multiplier in two different solutions.

In Fig. 1(A) the frequency multiplier utilizes an "analog" DLL with charge pump and voltage-controlled delay-line, and Fig. 1(B) shows an 'all-digital DLL', where the phase detector commands a digital counter to count up or count down, and the generated output controls a digitally-controlled delay-line. The analog version in Fig. 1(A) has potentially a better capability to generate clock phases with smaller phase errors and smaller jitter. On the other hand, the digital DLL in Fig. 1(B) does not require any high-precision analog circuit and signals (thus a more desirable and robust solution for on-chip integration) but it has limited accuracy due to the quantization of the delay, which leads to a best-case minimum phase error corresponding to +/- 1 LSB of the digital counter.

When the DLL (in Fig. 1(A) or in Fig. 1(B)) is locked, the delay-line generates different equally spaced clock phases within one clock period. The generated clock phases from the DLL are then used as inputs to a frequency multiplier block which generates the multiplied version of the reference clock. A possible implementation of frequency multiplier combines the edges of clock phases to generate multiplied frequency as shown in Figure 2.

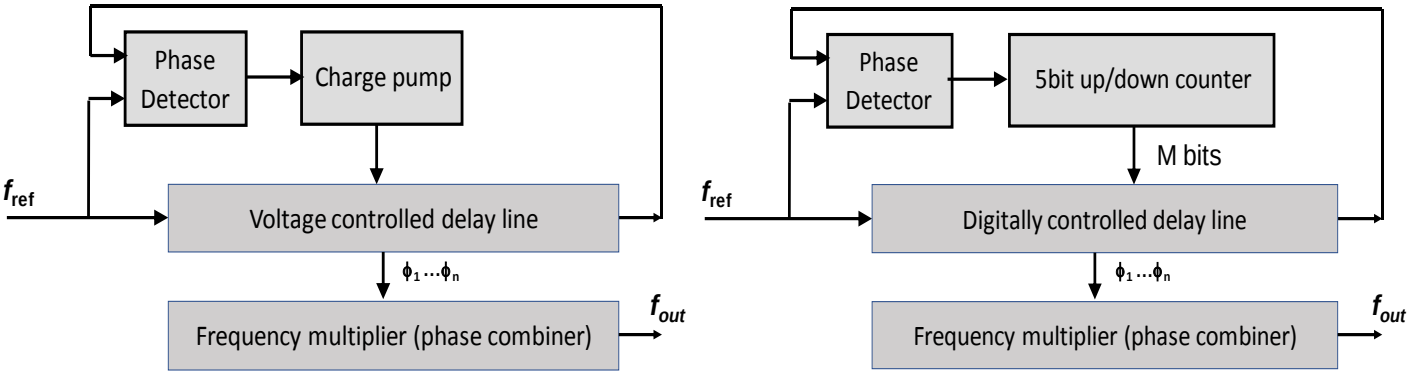

Fig. 1(A) **Fig. 1(B)**

Figure 1: System Block diagram of DLL-based frequency multiplier, using (A) DLL with charge pump and voltage-controlled delay-line. or (B) a fully digital solution with digital counter and digitally-controlled delay-line.

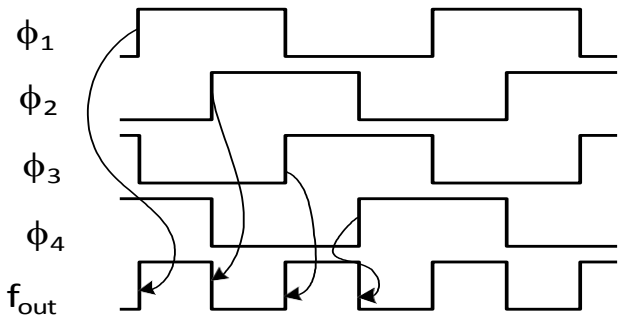

Figure 2: Example of frequency multiplication, here combining four clock phases to generate 2 X higher clock frequency (f_{out}).

3 Area and performance requirements

The table below summarizes the performance requirements. Each requirement has its number, formulated text, and the given degree of priority. Three degrees of priority are used: high, medium, and low. High is a firm requirement with no possibility of relaxation, while medium requirements can be relaxed somewhat after good motivation.

Requirement	Requirement text	Priority
1	Design for low power	Medium
2	Integrate as many system components as possible on-chip	High
3	Schematic and layout must be verified by simulation	High
4	On-chip evaluation should be implemented for full speed testing	High
5	Multiplied clock frequency at nominal supply (3.3V) >1 GHz	High
6	Simulated chip power consumption < 100mW (3.3V supply)	Medium
7	Simulated circuit power (normal activity) < 50mW (3.3V supply)	Medium
8	Maximum transistor sizing = 20µm	Medium
9	Chip core area < 0.27mm^2	High
10	Total project pin count: 12	High
11	Design technology is AMS 4-Metal 0.35 □m CMOS	High
12	The most important system nodes should have off-chip access pins	Medium
13	On-chip current densities < 1 mA/□m	High
14	All requirements fulfilled in “typical”, “slow”, and “fast” process corners and for temperatures between 25 and 110 ^{o}C	Medium

4 Available Resources

- Material given by the supervisor
- IEEE Xplore digital library, http://ieeexplore.ieee.org/, access given through LiU

Tools

- Circuit simulation and layout tools from Cadence, http://www.cadence.com/

References

- J.M. Rabaey, A. Chandrakasan, and B. Nikolic, Digital Integrated Circuits, 2nd ed., Prentice Hall, 2003, ISBN 0-13-120764-4.
- B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, 2nd edition, 2016.
- N. Waste and K. Eshraghian, “Principles of CMOS VLSI Design”, Addison-Wesley, 1993.
- S.-M. Kang and Y. Leblebici, “CMOS Digital Integrated Circuits: Analysis and Design”, McGraw-Hill, 1999.

For more literature references consult with your supervisor.