VLSI Chip Design Project TSEK06

Project Description and Requirement Specification

Version 1.2

Project: Direct VCO, 300 MHz/100 MHz, Programmable PLL
Extended to: 10 dBm modulating FM transmitter (Optional)

Project number: 4

Project Group:

Name	Project members	Telephone	E-mail
	Project leader & designer 1(6)		
	Designer 2(6)		
	Designer 3(6)		
	Designer 4(6)		
	Designer 5(6)		
	Designer 6(6)		

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1 Background

This document describes the design requirement specification of a direct VCO modulating FM Radio Transmitter. This simple transmitter can link your home entertainment system to a portable FM radio receive. For example, you can play a CD in your living room and listen to it on a portable radio in back yard.

1.1 Project Goal

The project goal is to design an integrated circuit (IC) in complementary metal-oxide semiconductor (CMOS) technology. Students, participating in this project as project members and project leaders, should learn the different steps of the IC design flow. That includes the given system architecture analysis, simulation, layout implementation and verification. The project students have an optional choice to manufacture the designed IC circuit on a chip. To test the manufactured chips, another course (TSEK11) is available after the project.

1.2 Milestones and Deadline

1	**Project selection**	**January 17**
2	Pre-study, project planning, and discussion with supervisor	Week 4
3	High-level modeling design and simulation result (report)	February 6
4	Gate/transistor level design and simulations result (report)	March 8
5	Layout, DRC, parasitic extraction, LVS, post-layout simulations, modification and chip evaluations.	May 1
6	**DEADLINE** Delivery of the completed chip.	**May 3**
7	**DEADLINE**, Final report, and oral presentation	**May 18**

1.3 Parties

The following parties are involved in this project:

- Customer: Yonatan Kifle
- Project supervisor: Yonatan Kifle

Tasks:

1. Formulates the project requirements
2. Provides technical support
3. Reviews the project documents.

- Project leader: One of the members in the design team.

Tasks:

- Responsible for organization of the team and the project planning.

- Divides the design and documentation work in an efficient way
- Organizes the team meetings as well as the meetings between the team and supervisor
- Keeps the supervisor informed about the progress of the project (**at least one email or meeting per week**)

• Project design members (including the project leader)

1 Are equally responsible for project planning and design.
2 Participate actively in all the meetings
3 Support the team and the project leader
4 Keep the team and project leader informed about the progress of their tasks.

2 Project Description

2.1 System Description

The system block level diagram is shown in Error: Reference source not found. The complete system to be built should include the phase-frequency detector, off-chip low pass filter (LPF), VCO (e.g. current steering amplifier based or current starved inverter based voltage controlled oscillator), programmable divider (divide by 4 and divide by 12) and optional blocks of power amplifier, pre-emphasis circuit, and on-chip audio amplifier. The off-chip components include microphone coupling circuit and matching circuit (if needed) for antenna.

The core of transmitter is VCO whose center frequency can be controlled by controlling the current through CSA (Current Steering Amplifier) or the current through current-starved inverter cells. This VCO do not need on-chip capacitor or inductor, although its phase noise performance is not as good as conventional VCO using inductor and varactors.

If the project progress and interest of the participants allow the project to include the audio and power amplifers the following information will be useful. A linear class A amplifier is one candidate for this application (Razavi, RF Micro., Chap-12). However, a simple output buffer (class D) might also be used as the power amplifier in this case. The matching circuit can be resistor-capacitor circuit for simplicity. The more efficient matching circuits employ both L and C components. The MIC is Electret Microphone with SNR better than 50dB. The headphone-mic set used with sound card of PC can also be used.

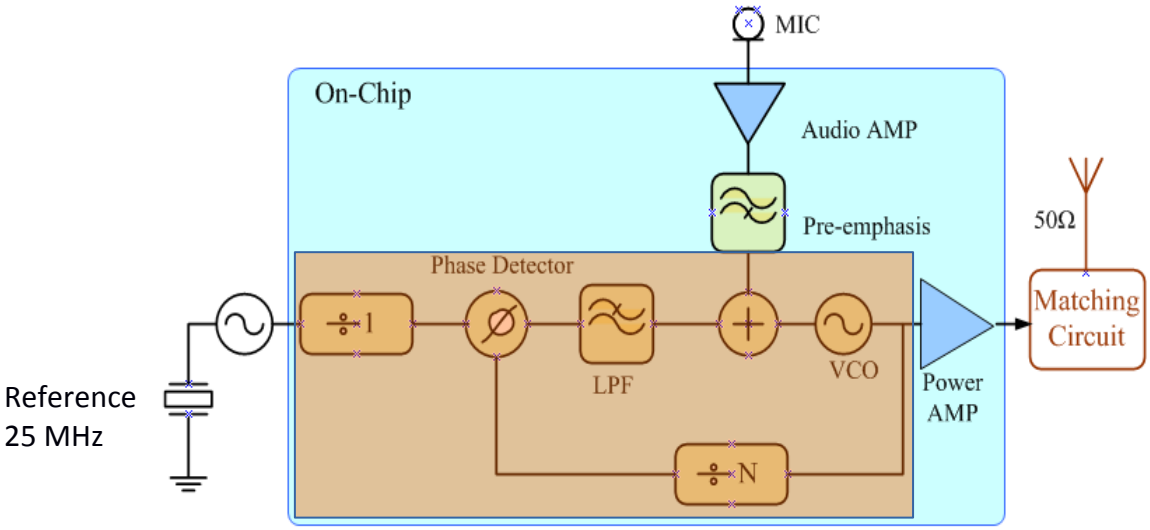

Figure 1: System Block diagram of 100 MHz, 10 dBm direct VCO modulating FM radio Transmitter.

2.2 Important Design Metrics

Power Supply	3.3 V ±5%
Transmitter Frequency	100 MHz – 300 MHz
Output Power	10 dBm (10 mW)
Total Power Consumption	≤ 100 mW
Audio Input Sensitivity	0.5 V_{rms} for +/- 75 kHz
Spurious Emissions	Better than -45 dBc (with ref to carrier)
Modulation Frequency	100 Hz – 5 kHz (Audio)
Frequency Deviation	± 75 kHz

NOTE – Most countries accept emission of 10 dBm in FM band including Sweden. So the maximum output power of transmitter is limited to 10 dBm (10 mW). This will give more than 100-200 meters of range with clear reception using typical commercial FM receiver. This is solely an educational project and no approval from any regulation agency is required to build and test this transmitter for educational purposes.

3 Area and Performance Requirements

The table below summarizes the circuit performance requirements. Each requirement has its number, formulated text, and the given degree of priority. Three degrees of priority are used: high, medium, and low. High is a firm requirement with no possibility of relaxation, while medium requirements can be relaxed somewhat after good motivation.

Requirement	Requirement Text	Priority
1	Integrate as many components as possible on-chip	High
2	Schematic and layout must be verified by simulation	High
3	Simulated chip power consumption < 100 mW (3.3 V supply)	Medium
4	Maximum transistor sizing < 200 µm	Medium
5	Chip core area < 0.27 mm^2	High
6	Total project pin count: 12	High
7	Design technology is AMS 4-Metal 0.35-µm CMOS	High
8	The most important system nodes should have off-chip access pins	Medium
9	On-chip current densities < 1 mA/µm	High
10	All requirements fulfilled in “typical”, “slow”, and “fast” process corners and for temperatures between 25 and 110 ^oC	Medium
11	Power supply decoupling capacitors	High

4 Available Resources

- Material given by the supervisor
- IEEE Xplore digital library, http://ieeexplore.ieee.org/, access given through LiU

4.1 Tools

- Circuit simulation and layout tools from Cadence®, http://www.cadence.com/

4.2 References

- Howard.C.Yang, "A Low Jitter 0.3-165 MHz CMOS PLL Frequency Synthesizer for 3 V/5V operation", IEEE J of Solid State, 1997, Vol.32
- Behzad Razavi, "Design of Analog CMOS Integrated Circuits", McGraw-Hill ISBN: 9780071188395 (PLL and CMOS amplifier Chapters)
- Behzad Razavi, "RF Microelectronics", Prentice Hall PTR, ISBN or 0132839415/9780132839419, 2012, (PLL, Power Amplifiers and Transmitter Chapters)

It is highly recommended that students taking this project also take the course TSEK02 and TSEK03.

For more literature references consult with your supervisor.