VLSI Chip Design Project TSEK06

Project Description and Requirement Specification

Version 1.1

Project: A 16-Bit Kogge-Stone Adder

Project number: 3

Project Group:

Name	Project members	Telephone	E-mail
	Project leader and designer 1(5)		
	Designer 2(5)		
	Designer 3(5)		
	Designer 4(5)		
	Designer 5(5)		

Customer and Supervisor: Martin Nielsen-Lönn
Office: B-house 3D:535, Phone: 013-28 89 46
Email: martin.nielsen.lonn@liu.se

1 Background

This document describes the design requirement specification of a 16-bit Kogge-Stone (KS) Adder. The KS-adder utilizes a parallel-prefix topology to reduce the critical path in the adder. The critical path, which is the carry generation path, has a logarithmic dependence of the bit-width. This should be compared to the linear dependence in the ripple carry adder. There are many ways to implement the carry generation tree for parallel prefix adders, but KS implementation is the most straightforward, and also it has one of the shortest critical paths of all tree adders. The drawback with the KS implementation is the large area consumed and the somewhat complex routing of interconnects.

1.1 Project Goal

The project goal is to design an integrated circuit (IC) in complementary metal-oxide semiconductor (CMOS) technology. Students, participating in this project as project members and project leaders, should learn the different steps of the IC design flow. That includes the given system architecture analysis, simulation, layout implementation and verification. The project students have an optional choice to manufacture the designed IC circuit on a chip. To test the manufactured chips, another course (TSEK11) is available after the project.

1.2 Milestones and Deadline

1	Project selection	January 17
2	Pre-study, project planning, and discussion with supervisor	Week 4
3	High-level modeling design and simulation result (report)	February 6
4	Gate/transistor level design and simulations result (report)	March 8
5	Layout, DRC, parasitic extraction, LVS, post-layout simulations, modification and chip evaluations.	May 3
6	**DEADLINE** Delivery of the completed chip.	**May 18**
7	**DEADLINE**, Final report, and oral presentation	**May 18**

1.3 Parties

The following parties are involved in this project:

1. Customer: Martin Nielsen-Lönn
2. Project supervisor: Martin Nielsen-Lönn

   Tasks:

   - Formulates the project requirements
   - Provides technical support
   - Reviews the project documents.
3. Project leader: One of the members in the design team.

   Tasks:

- Responsible for organization of the team and the project planning.
- Divides the design and documentation work in an efficient way
- Organizes the team meetings as well as the meetings between the team and supervisor
- Keeps the supervisor informed about the progress of the project (**at least one email or meeting per week**)

4. Project design members (including the project leader)
   - Are equally responsible for project planning and design.
   - Participate actively in all the meetings
   - Support the team and the project leader
   - Keep the team and project leader informed about the progress of their tasks.

2 Project Description

2.1 System Description

The complete system to be built should include the adder, on-chip evaluation circuits, and I/O circuitry. Because of the limited amount of pads a bit serial-to-parallel input/output interface (SPI) must be used to feed input vectors to the adder. The total system block level is shown in Figure 1.

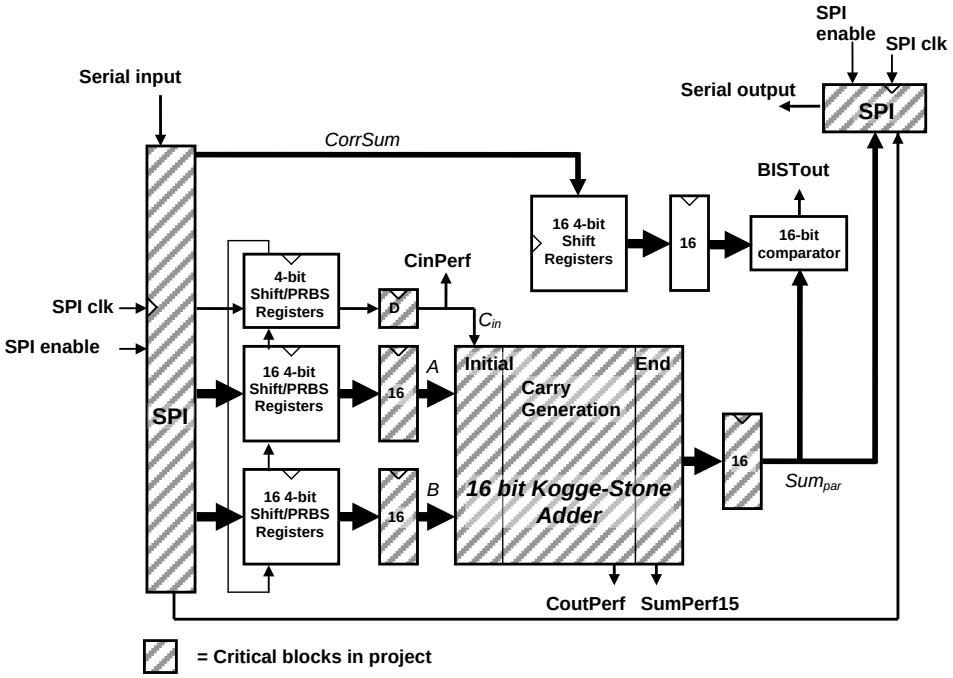

Figure 1: System Block diagram of Adder and evaluation circuitry.

The inputs are feed to the circuit in a bit-serial data stream and are converted into 16-bit vectors by the serial to parallel converters. Four different test vectors for input ***A***, ***B***, and C_{in} respectively are feed into the 4-bit shift registers on-chip. The correct sum vectors (***CorrSum***) are feed into the 4-bit shift registers. With the four test vectors a full speed on-chip evaluation is possible through the comparator circuitry, which outputs a signal that indicate if the counter evaluated the input data correct or not (***BISTOUT***). Power measurements of the adder are done using PRBS data at the input of the adder. Outputs of the sum vector are possible

through a parallel-to-serial interface (***Sum_{par}***). The MSB and the carry output are also feed out of the chip for full-speed performance measurements (***CoutPerf, SumPerf15***).

2.2 Important Design Metrics

The adder should be designed for ultra-low power. The aim is to reach correct functionality from nominal power-supply (3.3 V) down to sub-threshold operation; that is the power supply voltage should be lower than the threshold voltage of the transistor. At nominal power supply the performance of the adder should be maximized reaching at least a minimum operational frequency of 200 MHz. In the sub-threshold operation no requirement on minimum operational frequency is given however, the adder should have full functionality.

3 Area and Performance Requirements

The table below summarizes the circuit performance requirements. Each requirement has its number, formulated text, and the given degree of priority. Three degrees of priority are used: high, medium, and low. High is a firm requirement with no possibility of relaxation, while medium requirements can be relaxed somewhat after good motivation.

Requirement	Requirement Text	Priority
1	Design for full functionality in sub-threshold operation	High
2	Integrate as many system components as possible on-chip	High
3	Schematic and layout must be verified by simulation	High
4	On-chip evaluation should be implemented, for full speed testing	High
5	Minimum clock-frequency at nominal supply (3.3 V) > 200 MHz	Medium
6	Minimum adder frequency at nominal supply (3.3 V) > 400 MHz	Medium
7	Simulated chip power consumption < 100 mW (3.3 V supply)	Medium
8	Simulated adder power (normal activity) < 50 mW (3.3 V supply)	Medium
9	Maximum transistor width in the adder circuitry = 20 µm	Medium
10	Chip core area < 0.27 mm^2	High
11	Total project pin count <= 12	High
12	Design technology is AMS 4-Metal 0.35-µm CMOS	High
13	The most important system nodes should have off-chip access pins	Medium
14	On-chip current densities < 1 mA/µm	High
15	All requirements fulfilled in *"typical"*, *"slow"*, and *"fast"* process corners and for temperatures between 25°C and 110°C	Medium

4 Available Resources

- Material given by the supervisor
- IEEE Xplore digital library, http://ieeexplore.ieee.org/, access given through LiU

4.1 Tools

- Circuit simulation and layout tools from Cadence®, http://www.cadence.com/

4.2 References

- J.M. Rabaey, A. Chandrakasan, and B. Nikolic., “Digital Integrated Circuits”, 2nd ed., Prentice Hall, 2003, ISBN 0-13-120764-4.
- N. Waste and K. Eshraghian, “Principles of CMOS VLSI Design”, Addison-Wesley, 1993.
- S.-M. Kang and Y. Leblebici, “CMOS Digital Integrated Circuits: Analysis and Design”, McGraw-Hill, 1999.
- B. Parhami, “Computer Arithmetic”, Oxford University Press, 2000.

For more literature references consult with your supervisor.