VLSI Chip Design Project TSEK06

Project Description and Requirement Specification

Version 0.1

Project: Piezoelectric energy harvesting

Project number: 5

Project Group:

Name	Project members	Telephone	E-mail
	Project leader and designer 1(5)		
	Designer 2(5)		
	Designer 3(5)		
	Designer 4(5)		
	Designer 5(5)		

Customer and Supervisor: Pavel Angelov
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1 Background

Energy Harvesting has increased in popularity both in products and in research the last decade. The idea is to collect energy from an ambient energy source therefore increasing the battery life of the system or perhaps remove the battery completely. Common ambient energy sources are solar, radio, temperature, and movement. In this project we are interested in vibration energy harvesting since it is useful in many different applications.

1.1 Project Goal

The project goal is to design an integrated circuit (IC) in complementary metal-oxide semiconductor (CMOS) technology. Students, participating in this project as project members and project leaders, should learn the different steps of the IC design flow. That includes the given system architecture analysis, simulation, layout implementation and verification. The project students have an optional choice to manufacture the designed IC circuit on a chip. To test the manufactured chips, another course (TSEK11) is available after the project.

1.2 Milestones and Deadline

1	Project selection	January 18
2	Pre-study, project planning, and discussion with supervisor	Week 4
3	High-level modeling design and simulation result (report)	February 17
4	Gate/transistor level design and simulations result (report)	March 17
5	Layout, DRC, parasitic extraction, LVS, post-layout simulations, modification and chip evaluations.	May 19
6	**DEADLINE** Delivery of the completed chip.	**May 24**
7	**DEADLINE**, Final report, and oral presentation	**May 29**

1.3 Parties

The following parties are involved in this project:

1. Customer: Pavel Angelov
2. Project supervisor: Pavel Angelov

   Tasks:

   - Formulates the project requirements
   - Provides technical support
   - Reviews the project documents.
3. Project leader: One of the members in the design team.

   Tasks:

   - Responsible for organization of the team and the project planning.
   - Divides the design and documentation work in an efficient way

- Organizes the team meetings as well as the meetings between the team and supervisor
- Keeps the supervisor informed about the progress of the project (**at least one email or meeting per week**)

4. Project design members (including the project leader)
   - Are equally responsible for project planning and design.
   - Participate actively in all the meetings
   - Support the team and the project leader
   - Keep the team and project leader informed about the progress of their tasks.

2 Project Description

2.1 System Description

A common method to extract energy from vibrations is to utilize the piezoelectric effect. By having a cantilever which moves with the vibrations and a piezoelectric film over it, charge is generated when the film is stretched. This charge can then be accumulated and used to power the main system.

Piezoelectric materials are constantly being improved but they still suffer from large parasitics. So the goal in this project is to cancel that parasitic as much as possible.

Figure 1 shows a block level system diagram.

The cantilever with its piezoelectric film generates a current proportional to the vibration which excites it. If the vibration frequency is close to the resonance frequency a sinusoidal current will be generated by the PEH. Due to the parasitic capacitance in parallel with the PEH the voltage will be phase shifted compared to current and just a small amount of power can be extracted from it using a normal rectifier.

One way of solving this is to detect when the current is crossing zero, equivalent to when the voltage is the highest, and resonate the parasitic capacitance with an inductor. This will flip the voltage over the PEH and make the current and voltage to go in phase. Thus a higher amount of energy can be extracted from the PEH.

The system contains 4 main blocks: rectifier, voltage/current measurement, drivers, and logic. To convert the AC input voltage to a more useable DC voltage a rectifier is needed, this can be either passive or synchronized. A vital part in this project is the logic and voltage/current measurement which is responsible for starting the bias-flip and the correct time and also stop it when the voltage has been flipped.

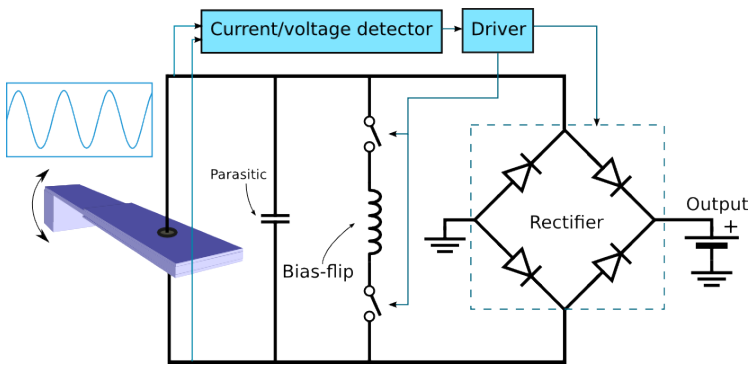

Figure 1: System Block diagram of vibration energy harvesting interface circuit with bias-flip.

3 Area and Performance Requirements

The table below summarizes the circuit performance requirements. Each requirement has its number, formulated text, and the given degree of priority. Three degrees of priority are used: high, medium, and low. High is a firm requirement with no possibility of relaxation, while medium requirements can be relaxed somewhat after good motivation.

Requirement	Requirement Text	Priority
1	Integrate as many components as possible on-chip	High
2	Schematic and layout must be verified by simulation	High
3	Chip core area < 0.27 mm^2	High
4	Output voltage > 2 V	High
5	Output current > 10 µA	High
6	Total project pin count: 12	High
7	Design technology is AMS 4-Metal 0.35-µm CMOS	High
8	The most important system nodes should have off-chip access pins	High
9	On-chip current densities < 1 mA/µm	High
10	All requirements fulfilled in “typical”, “slow”, and “fast” process corners and for temperatures between 25 and 110 ^oC	Medium

4 Available Resources

- Material given by the supervisor
- IEEE Xplore digital library, http://ieeexplore.ieee.org/, access given through LiU

4.1 Tools

- Circuit simulation and layout tools from Cadence®, http://www.cadence.com/

4.2 References

- Yogesh K. Ramadass, “An Efficient Piezoelectric Energy Harvesting Interface Circuit Using a Bias-Flip Rectifier and Shared Inductor (IEEE Journal of Solid-State Circuits Volume: 45, Issue: 1, Jan. 2010)
- Behzad Razavi, "Design of Analog CMOS Integrated Circuits", McGraw-Hill ISBN: 9780071188395

It is highly recommended that students taking this project also take the course TSEK37.

For more literature references consult with your supervisor.