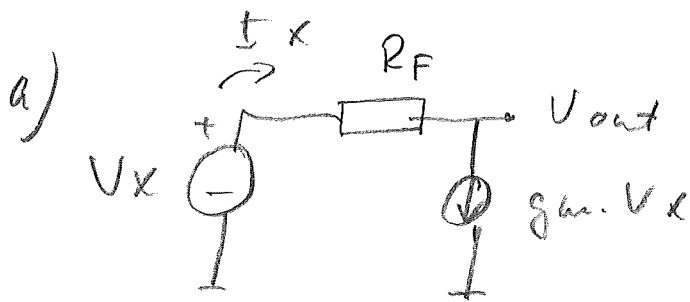


1. See Tutorial 1, problem 4

2. Small signal model



Small signal model
for R_{in} .

$$\bar{i}_X = g_m \cdot V_X \quad \underline{\underline{R_{in} = \frac{V_X}{\bar{i}_X} = \frac{1}{g_m}}}$$

b) Gain from point X: $\frac{V_{out} - V_X}{R_F} + g_m \cdot V_X = 0$

\Leftrightarrow

$$\frac{V_{out}}{V_X} = 1 - g_m \cdot R_F$$

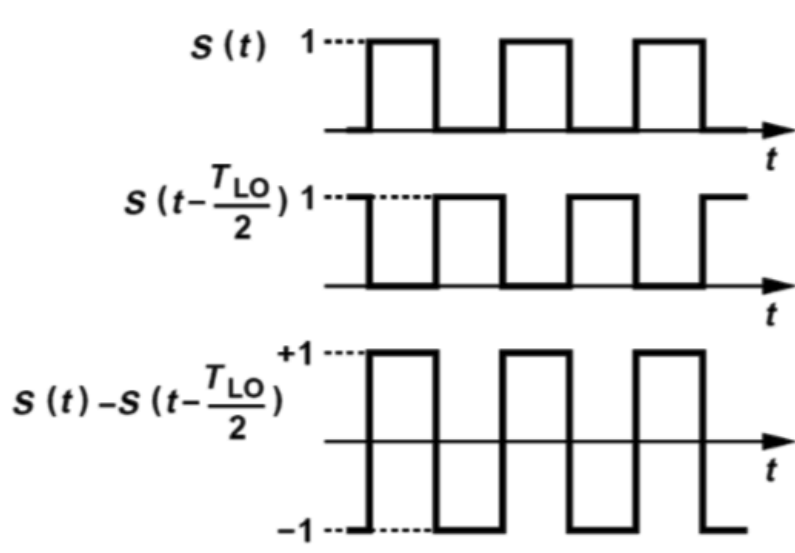
$$V_X = \frac{V_{s_n}}{V_{s_n} + R_s} \cdot \bar{v}_{in} \Rightarrow A_v = \frac{V_{out}}{\bar{v}_{in}} = \frac{1}{\frac{V_{s_n}}{V_{s_n} + R_s}} \cdot (1 - g_m \cdot R_F)$$

$$= \frac{1}{2} \left(1 - \frac{R_F}{R_s} \right) \quad R_F = 25R_s \Rightarrow A_v = \frac{1}{2} \left(1 - \frac{25}{1} \right) = \underline{\underline{-12}}$$

c) $\overline{V_{n,out}^2} = 4kTR_s \cdot A_v^2 = 4kTR_s \cdot \frac{1}{4} \left(1 - \frac{R_F}{R_s} \right)^2$

If $R_F = 25R_s \Rightarrow \overline{V_{n,out|R_s}^2} = 4 \cdot kTR_s \cdot (-12)^2 = \underline{\underline{576kTR_s}}$

3.



$$V_{out}(t) = I_{RF}R [S(t) - S(t - T_{LO}/2)] = I_{RF}R \cdot \frac{4}{\pi} \cos(\omega_{LO}t) + \dots$$

If $V_{RF} = A_{RF} \cos(\omega_{RF}t)$, then by ignoring the higher order terms:

$$V_{out}(t) = \frac{4}{\pi} g_{m3} R A_{RF} \cos(\omega_{RF}t) \cos(\omega_{LO}t)$$

$$\rightarrow V_{IF} = \frac{2}{\pi} g_{m3} R A_{RF} \cos((\omega_{RF} - \omega_{LO})t)$$

Therefore the conversion gain is:

$$G_C = \frac{V_{IF}}{A_{RF}} = \frac{2}{\pi} g_{m3} R$$

4. Please provide short answers (no motivations are needed) to the following questions:

a) For a well-designed transistor, is the gate noise is higher or lower than the channel noise? (0.5 p)

Higher. Book section 2.3.4.

b) What is the noise figure of noiseless mixer ("single-sideband noise)? (0.5 p)

3 dB. Book section 6.1.2.

c) When the colleagues discuss "fractional spurs" in the coffee room, what kind of circuit and variant are most likely discussed? (0.5 p)

Fractional-N synthesizers. Book section 11.1.

d) A class-C power amplifier can reach 100 % efficiency. Wow! What's the catch? (catch = "a hidden problem or disadvantage in an apparently ideal situation") (0.5 p)

The output power goes to zero. Book section 12.2.3.

The linearity is also bad, but it would still be usable => not really right answer...

e) If a well-designed inductor has a Q-value of 10 in the WLAN 802.11ac 5 GHz band, estimate the Q when this inductor is used in the WLAN 802.11n 2.4 GHz band. (0.5 p)

4.8. Book chapter 7, e.g. section 7.2.5.

f) Why are three-point oscillators less popular in RFIC design than cross-coupled oscillators? (0.5 p)

Tough startup condition, $g_m R_p > 4$. Single-ended. Book section 8.4.

5.

a. closed-loop transfer function

$$F(s) = \frac{\frac{1}{sC_1}}{\frac{1}{sC_1} + R_1} = \frac{1}{sR_1C_1 + 1}$$

The close loop Transfer Function:

$$\varphi_{out} = \frac{K_{VCO}K_{PD}}{s} \left(\varphi_{in} - \frac{\varphi_{out}}{M} \right) \left(\frac{1}{sR_1C_1 + 1} \right)$$

$$\frac{\varphi_{out}}{\varphi_{in}}(s) = \frac{K_{VCO}K_{PD}M}{s(sR_1C_1 + 1)M + K_{VCO}K_{PD}}$$

$$= \frac{K_{VCO}K_{PD}M}{s^2R_1C_1M + sM + K_{VCO}K_{PD}} = \frac{\frac{K_{VCO}K_{PD}}{R_1C_1}}{s^2 + s\frac{1}{R_1C_1} + \frac{K_{VCO}K_{PD}}{R_1C_1M}} = \frac{\frac{K_{VCO}K_{PD}}{R_1C_1}}{s^2 + 2\xi\omega_n s + \omega_n^2}$$

b. damping factor ζ

$$\xi = \frac{1}{2} \sqrt{\frac{\omega_{LPF} M}{K_{VCO} K_{PD}}}$$

c. natural frequency ω_n

$$\omega_n = \sqrt{\frac{K_{VCO} K_{PD} \omega_{LPF}}{M}}$$

d. loop bandwidth = $\zeta * \omega_n = 1/2 * \omega_{LPF} = 1 / (2RC)$.

6. a) 24 dBm average, PAIR = 5 dB, network losses = 1.5 dB \Rightarrow 24 + 5 + 1.5 = 30.5 dBm peak power.

$$30.5 \text{ dBm } (\approx 1 \text{ W}) = \underline{\underline{1.122 \text{ mW}}}$$

b) $P = \frac{V_p^2}{2R_L}$ where $V_p \approx V_{DD}$ (simplest approx.)

$$\Leftrightarrow R_L = \frac{V_p^2}{2P} \quad V_p = V_{DD} = 1.8 \text{ V}$$

$$P = 1.122 \text{ W}$$

$$\Rightarrow R_L = 1.4 \Omega$$

[Transformation ratio = $\frac{50 \Omega}{1.4 \Omega} = 35 \times$, not

so easy to do, generally ratio should not be larger than 10.]

c) Cascode gives possibility of higher supply voltage.

Linear PA \Rightarrow V_x may reach $2 \times V_{DD}$

65 nm CMOS (as an example); each transistor can safely handle $\sim 1.8 \text{ V} \Rightarrow$ cascode

(although usually not evenly distributed over the two transistors).