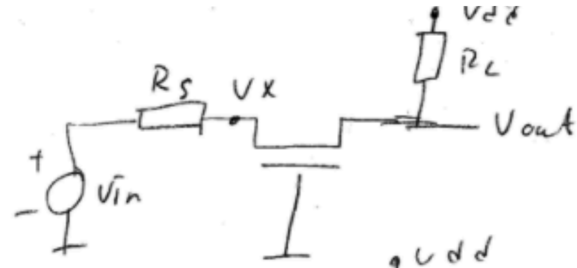
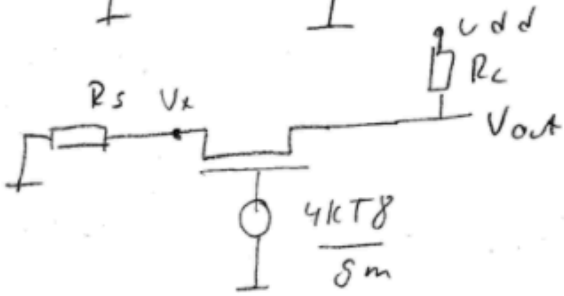
Solutions

(a) Circuit:



For noise



i) Gain? $\frac{V_{out}}{V_x} = g_m \cdot R_L$

$$A_v = \frac{V_{out}}{V_{in}} = g_m \cdot R_L \left(\frac{\frac{1}{g_m}}{\frac{1}{g_m} + R_s} \right) = g_m \cdot R_L \left(\frac{1}{1 + g_m \cdot R_s} \right)$$

When used as an LNA, select $g_m = \frac{1}{R_s} \Rightarrow$

$$A_v = \frac{R_L}{2R_s}$$

ii) Noise from M1: $\overline{V^2_{n,out\,M1}} = \frac{4kT\gamma}{g_m} \cdot \left(\frac{R_L}{R_s + \frac{1}{g_m}} \right)^2 = kT\gamma \frac{R_L^2}{R_s}$

Noise from R_L = $\overline{V^2_{n,out,R_L}} = 4kTR_L$

iii) NF: $1 + \frac{\overline{V^2_{n,out,M1}} + \overline{V^2_{n,out,R_L}}}{A_v^2 \cdot \overline{V^2_{n,R_s}}} =$

(1 a) cont.

$$= 1 + \frac{kT\gamma \frac{R_L^2}{R_s} + 4kTR_L}{\left(\frac{R_L}{2R_s}\right)^2 \cdot 4kTR_s} = 1 + \frac{}{kT\frac{R_L^2}{R_s}} =$$

$$= \boxed{1 + \gamma + 4\frac{R_s}{R_L}} \quad NF$$

1 b) For gate noise, add another voltage source on the gate: $\overline{V_{n\,out,M1_G}^2} = \frac{4kTR_G}{3} \cdot \left(\frac{R_L}{2R_s}\right)^2 =$

$$= \frac{kT \cdot R_G \cdot R_L^2}{3R_s^2}$$

$$\Rightarrow NF = 1 + \frac{kT\gamma \frac{R_L^2}{R_s} + \frac{kTR_G \cdot R_L^2}{3R_s^2} + 4kTR_L}{kT\frac{R_L^2}{R_s}} =$$

$$\boxed{1 + \gamma + \frac{R_G}{3R_s} + 4\frac{R_s}{R_L}} \quad NF$$

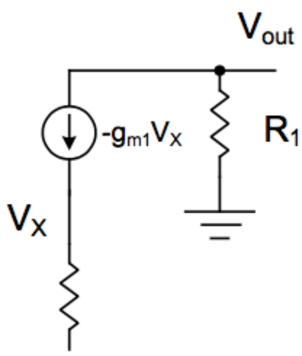
1c.

3 dB, see Razavi, chapter 6.1.2

2.

As a start, see Tutorial 6, problem 2. <u>But here not matched, gm ≠ Rs.</u> This is actually Problem 5.8 from the book.

1. Calculate the votlage gain



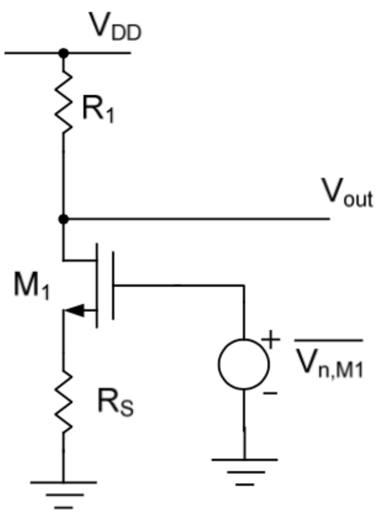
$$V_{out} = g_{m1} V_X R_1 \qquad \rightarrow \qquad A_X = \frac{V_{out}}{V_X} = g_{m1} R_1$$

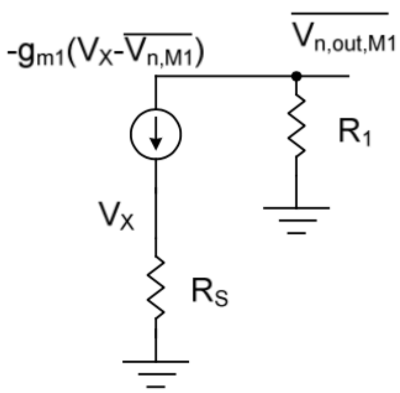
Since $R_{in} = \dfrac{1}{g_{m1}}$, we have the voltage gain from Vin to Vout:

$$A_V = \frac{\dfrac{1}{g_{m1}}}{R_S + \dfrac{1}{g_{m1}}} A_X = \frac{g_{m1} R_1}{1 + R_S g_{m1}}$$

2. Calculate noise figure
   The noise contributions are from M1, R1, and Rs.

   a. Calculate output noise from M1





2. (continued)

$A_{M1} = -\dfrac{R_1}{R_S + \dfrac{1}{g_{m1}}}$, hence the output noise of M1 can be obtained from

$$\left.\overline{V_{n,out}^2}\right|_{M1} = \frac{4kT\gamma}{g_{m1}} A_{M1}^2 = \frac{4kT\gamma}{g_{m1}} \left(\frac{R_1}{R_S + \frac{1}{g_{m1}}}\right)^2$$

b. Calculate output noise from R1

$$\left.\overline{V_{n,out}^2}\right|_{R_1} = 4kTR_1$$

The noise of R_S is multiplied by the gain when referred to the output, and the result is divided by the gain when referred to the input.

We thus have:

$$NF = \frac{1}{4kTR_S} \frac{\overline{V_{n,out}^2}}{A_V^2}$$

$$= 1 + \frac{4kTR_1}{4kTR_S\left(\frac{g_{m1}R_1}{1+R_S g_{m1}}\right)^2} + \frac{\frac{4kT\gamma}{g_{m1}}\left(\frac{R_1}{R_S + \frac{1}{g_{m1}}}\right)^2}{4kTR_S\left(\frac{g_{m1}R_1}{1+R_S g_{m1}}\right)^2}$$

$$= 1 + \frac{(1+R_S g_{m1})^2}{R_S R_1 g_{m1}^2} + \frac{\gamma}{g_{m1} R_S}$$

3.

a. See Example 5.3 in Razavi. New value for Q = 5400/(5900-4900) = 5.4
b. On-chip L:s are usually much more lossy than on-chip C:s.
c. In the L, the Q value is mainly limited by the series resistance in the metallization and, at higher frequencies, the losses in the substrate.

4.

(a) DC phase shift = 180° (frequency → 0)

Open loop circuit contains one pole

=> Frequency dependent phase shift = 90° (at frequency → ∞)

Total phase shift = 90° + 180° = 270° => No oscillation.

(b) DC phase shift = 0° (frequency → 0)

Open loop circuit contains two poles

=> Frequency dependent phase shift = 90° + 90° = 180° (at frequency → ∞)

Total phase shift = 0° + 180° = 180° => No oscillation.

(c) DC phase shift = 180° (frequency → 0)

Open loop circuit contains two poles

=> Frequency dependent phase shift = 90° + 90° = 180° (at frequency → ∞)

Total phase shift = 180° + 180° = 360°

But as frequency → ∞ the loop gain vanishes => No oscillation.

(d) DC phase shift = 180° (frequency → 0)

Open loop circuit contains three poles

=> Frequency dependent phase shift = 90° + 90° + 90° = 270° (at frequency → ∞)

Total phase shift = 180° + 270° = 450° or 90°

However at $f = f_{p1,2,3} < \infty$, where f_p is the cut-off frequency of a stage, the frequency dependent phase shift = 45° + 45° + 45° = 135°

Therefore for some $f_p < f < \infty$ the circuit may oscillate with a sufficient loop gain.

5.

(a) Ignoring higher frequency terms:

$$i_{LO}(t) = \frac{1}{2} + \frac{2}{\pi}\cos\omega_{LO}(t) - \frac{2}{3\pi}\cos 3\omega_{LO}(t) + \ldots \quad \text{and} \quad i_{RF}(t) = I_{RF}\cos\omega_{RF}(t) + I_{BIAS}$$

Therefore in case of switching the output voltage at IF is given by:

$$i_{IF}(t) = \left[I_{RF}\cos\omega_{RF}(t) + I_{BIAS}\right] \times \left[\frac{1}{2} + \frac{2}{\pi}\cos\omega_{LO}(t)\right]$$

$$i_{IF}(t) = \frac{I_{RF}}{2}\cos\omega_{RF}(t) + \frac{I_{BIAS}}{2} + \frac{2I_{BIAS}}{\pi}\cos\omega_{LO}(t) + \frac{I_{RF}}{\pi}\cos(\omega_{LO} - \omega_{RF})t$$

Applying $V_{IF}(t) = -g_m R V_{RF}$, The conversion gain is given by:

$$G_C = \left|\frac{V_{IF}(t)}{V_{RF}(t)}\right| = \left|\frac{R \times i_{IF}(t)}{\frac{i_{RF}(t)}{g_m}}\right| = \frac{\frac{1}{\pi} g_m R I_{RF}}{I_{RF}} = \boxed{\frac{1}{\pi} g_m R}$$

similar to *gm* for our transistors, since long channel devices

(b)

$$\overline{V}^2_{nout,M3} = \overline{I}^2_{n,M3} R^2 = 4KT\gamma g_{d0} R^2 \Delta f$$

$$\overline{V}^2_{nout,R_S} = \overline{V}^2_{n,R_S} A_V^2 = 4KTR_S (g_m R)^2 \Delta f$$

$$\overline{V}^2_{nout,R} = 4KTR\Delta f$$

The noise factor is given by:

$$F = \frac{\overline{V}^2_{nout,M3} + \overline{V}^2_{nout,R_S} + \overline{V}^2_{nout,R}}{(G_C)^2 \overline{V}^2_{n,R_S}} = \boxed{\pi^2\left(1 + \frac{\gamma}{g_m^2 R_S} + \frac{1}{g_m^2 R R_S}\right)}$$

6.

a. A Class-A has the best linearity among the linear classes (A, AB, B, C).
By DC-biasing it to half the full output signal, any frequency signal would just swing around this middle point, with no limitations (unless very large).
Class-B is off half the cycle, it is very non-linear.

b. A Class-A: see above.
Class-D is a switching amplifier, it has only on/off levels, and therefore very bad linearity.

c. AB Class-A has 50 % maximum theoretical efficiency, class-B 78.5 %, and the class AB somewhere between.

d. A Both class-A and class-E have voltage peaks (on the drain of the transistor above Vdd, but A no more than about 2, while class-E is over 3.5.

e. DE = RF-power out / DC power in.
PAE = (RF-power out - RF-power in) / DC power in

So PAE also takes into account the input power. With high gain, then DE >> PAE, with high gain DE ≈ PAE, but PAE can never be higher than the DE.

From the lecture notes:

- Drain (collector) efficiency [%] $$\eta_D = \frac{P_{RF}}{P_{DC}}$$
- Power-added efficiency [%] $$PAE = \frac{P_{RF} - P_{IN}}{P_{DC}}$$
- PAE can also be expressed as $$PAE = \eta_D \frac{G-1}{G}$$
- PAE: when gain is low, it takes some power to drive the PA, must be accounted for!