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EXAMINATION IN
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TSEK03
RADIO FREQUENCY INTEGRATED CIRCUITS

Date:	2014-03-20
Time:	8-12
Location:	U1
Aids:	Calculator, Dictionary
Teachers:	Behzad Mesgarzadeh (5719)
	Amin Ojani (2815)

12 points are required to pass.

12-16 : 3

16-20 : 4

20-24 : 5

Please start each new problem at the top of a page!
Only use one side of each paper!

1) The mean square thermal noise density of a resistor in the room temperature is $33 \times 10^{-17}\ \ V^2/Hz$. If this resistor is used in a first-order RC filter as shown in Fig. 1, and the noise bandwidth of the RC filter is $50\ \ MHz$, calculate the value of C in Fig.1. Present the details of your calculations. (4 p)

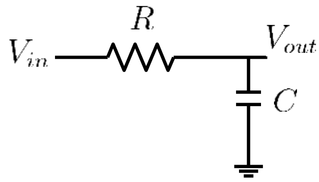

Fig. 1. A single-pole RC filter.

Hints:

i) Boltzmann's constant is $1.38 \times 10^{-23}\ \ J/K$

ii) $\int \frac{dx}{1+x^2} = \tan^{-1} x$

iii) Noise bandwidth: $\Delta f = \frac{1}{|H_{pk}|^2} \int_0^{\infty} |H(f)|^2\, df$

2) Input stage of a single-ended LNA is shown in Fig. 2. Assume that $C_{GS1} = 1$ pF , $L_1 = 1.6$ nH, and $\lambda = \gamma = 0$.

(a) Calculate the frequency at which the input impedance is purely resistive (a real value). (3 p)

(b) Calculate the transconductance of the transistor (g_{m1}), to match with a 50-Ω source resistance. (2 p)

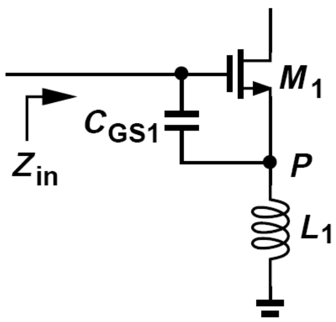

Fig. 2. Input stage of a single-ended LNA.

3) A single-balanced mixer is shown in Fig. 3. Ignore channel length modulation.

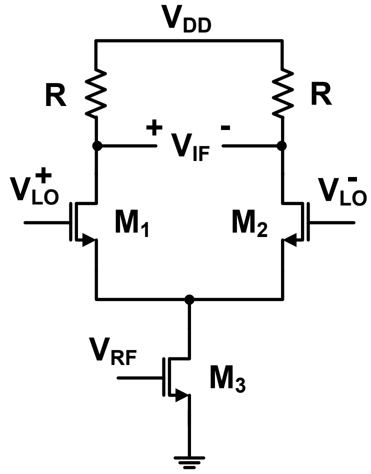

Fig. 3. A single-balanced mixer.

(a) If LO signal is a square wave toggling between 0 and 1 with 50% duty cycle and LO switching is abrupt, derive an expression for the conversion gain of this mixer.

(3 p)

(b) If LO signal is a sine wave varying between 0 and 1, drain currents of M_1 and M_2 will remain approximately equal for a period of ΔT in each half cycle reducing the conversion gain. If ΔT is 10% of the LO signal period, calculate the conversion gain reduction in dB.

(2 p)

Hint:

For a square wave LO signal toggling between -1 and 1:

$$V_{LO}(t) = \frac{4}{\pi}\cos\omega_{LO}(t) - \frac{4}{3\pi}\cos 3\omega_{LO}(t) + \frac{4}{5\pi}\cos 5\omega_{LO}(t) - \ldots$$

4) Figure 4 shows a unity gain feedback system with two identical ideal integrators. The transfer function of each integrator in Laplace domain is $H(s) = K/s$.

(a) Is this feedback system stable? Motivate your answer using Barkhausen criteria. (2 p)

(b) Write a differential equation describing this feedback system and solve it for X=0. Is this result consistent with your answer in part (a)? Why? (3 p)

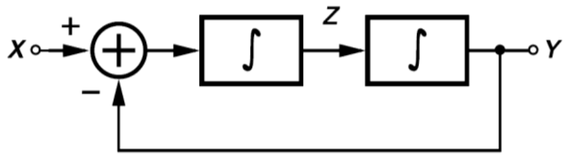

Fig. 4. Two ideal integrators inside a unity gain feedback.

5) Figure 5 shows a block level description of a PLL.

(a) Determine the closed-loop transfer function (i.e., $\frac{\Phi_{out}}{\Phi_{in}}(s)$) and the type of the PLL. (3 p)

(b) Prove that for slow input phase variations the output tracks the input. (2 p)

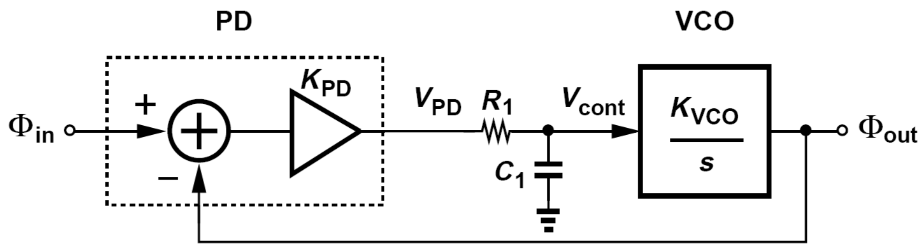

Fig. 5. Block diagram of a PLL.

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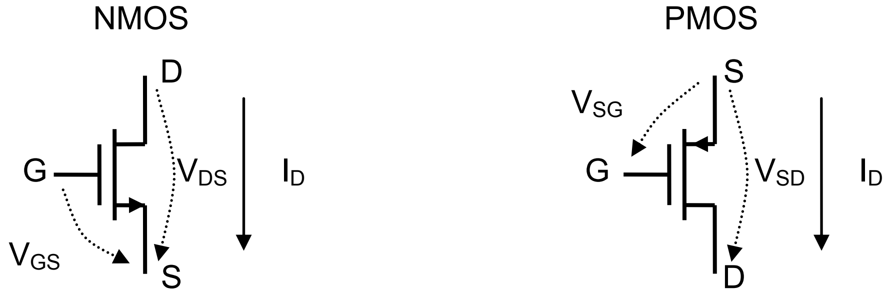
TRANSISTOR EQUATIONS



NMOS

- **Cutoff:** $I_D = 0$ $(V_{GS} < V_{TN})$
- **Linear mode:**

$$I_D = \mu_n C_{ox} \frac{W}{L}\left((V_{GS} - V_{TN})V_{DS} - \frac{V_{DS}^2}{2}\right) \quad (V_{GS} > V_{TN}) \text{ and } (V_{DS} < V_{GS} - V_{TN})$$

- **Saturation mode:**

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TN})^2(1 + \lambda V_{DS}) \quad (V_{GS} > V_{TN}) \text{ and } (V_{DS} > V_{GS} - V_{TN})$$

PMOS

- **Cutoff:** $I_D = 0$ $(V_{GS} < |V_{TP}|)$
- **Linear mode:**

$$I_D = \mu_p C_{ox} \frac{W}{L}\left((V_{SG} - |V_{TP}|)V_{SD} - \frac{V_{SD}^2}{2}\right) \quad (V_{GS} > |V_{TP}|) \text{ and } (V_{SD} < V_{SG} - |V_{TP}|)$$

- **Saturation mode:**

$$I_D = \frac{1}{2}\mu_p C_{ox} \frac{W}{L}(V_{SG} - |V_{TP}|)^2(1 + \lambda V_{SD}) \quad (V_{GS} > |V_{TP}|) \text{ and } (V_{SD} > V_{SG} - |V_{TP}|)$$