# **EXAMINATION IN**

### **TSEK03/TEN1**

## **RADIO FREQUENCY INTEGRATED CIRCUITS**

Date:	2013-06-05
Time:	14-18
Location:	TER3
Aids:	Calculator, Dictionary
Teachers:	Behzad Mesgarzadeh (5719)
	Amin Ojani (2716)

- 12 points are required to pass.
- 12-16:3

- 16-20:4
- 20-24:5

Please start each new problem at the top of a page! Only use one side of each paper!

(5 p)

1) Figure 1 shows an amplifier schematic. Determine the input-referred 1/f noise voltage. Ignore all the thermal noise sources. Assume  $g_m \gg 1/r_o$ ,  $\gamma = 0$ , and  $\lambda \neq 0$ .

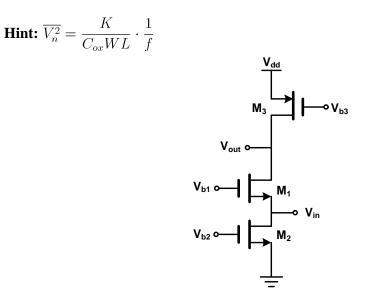


Fig. 1. An amplifier schematic.

2) Consider the wideband common-gate low noise amplifier (LNA) shown in Fig. 2.  $R_S$  is the input source resistance. Assume that the transistors are long-channel devices with  $\lambda_n = 0$ . Also assume that  $\gamma_{body effect} = 0$ .

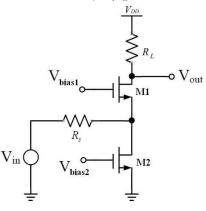


Fig. 2. A common-gate LNA.

- (a) Calculate the input impedance of the LNA. Assume that we can neglect all parasitics associated with the transistors. (2 p)
- (b) Derive an expression for the noise figure of the LNA. Only consider the thermal noise sources and ignore the gate noise of the transistors. Also assume that  $R_L$  is a noiseless resistor. (3 p)

**Hint:**  $\overline{i_{n,M}^2} = 4KT\gamma g_m$ 

**3**) The circuit shown in Fig. 3 is a dual-gate mixer used in traditional microwave design. Assume abrupt edges and a 50% duty cycle for the LO, and neglect channel-length modulation and body effect.

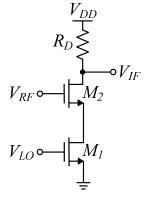
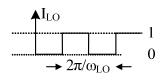


Fig. 3. A dual-gate mixer.

- (a) Assume that  $M_1$  is an ideal switch. Determine all the frequency components which appear at the mixer IF port. (2 p)
- (b) Assume when  $M_1$  is on, it has an on-resistance of  $R_{on1}$ . Compute the voltage conversion gain of the circuit. Assume  $M_2$  does not enter the triode region and denote its transconductance by  $g_{m2}$ . (1 p)
- (c) Assume that  $M_1$  is an ideal switch (noise contribution is zero). Derive the expression for the noise figure of the mixer. (2 p)

**Hints:** 



i) 
$$i_{LO}(t) = \frac{1}{2} + \frac{2}{\pi} \cos \omega_{LO}(t) - \frac{2}{3\pi} \cos 3\omega_{LO}(t) + \frac{2}{5\pi} \cos 5\omega_{LO}(t) - ...$$
  
ii)  $i_{RF}(t) = I_{bias} + I_{RF} \cos \omega_{RF}(t)$   
iii)  $\overline{i_{n,M}^2} = 4KT\gamma g_m$ 

- 4) A negative-resistance oscillator operating at 2.4 GHz frequency is shown in Fig. 4. The resonant circuit is implemented using inductor L = 5 nH with Q = 10 and a variable capacitor C. Assume that we can neglect all parasitics associated with the transistors.
- (a) What is the minimum width of two identical transistors  $M_1$  and  $M_2$  to ensure the oscillation? (2 p)
- (b) How much should the variable capacitance C be varied to enable tuning from 2.4 GHz to 2.5 GHz? (1 p)
- (c) For a capacitance corresponding to 2.4 GHz oscillation frequency, if an additional inductor of 5 nH is connected in parallel with the capacitor *C*, how much will the oscillation frequency change (in percentage)? (2 p)

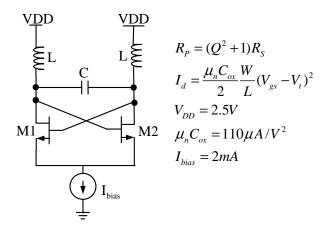


Fig. 4. A negative-resistance oscillator.

5) Figure 5 shows a block level description of a PLL.

(a) Determine the closed-loop transfer function (i.e.,  $\frac{\Phi_{out}}{\Phi_{in}}(s)$ ) and the type of the PLL. (2 p)

(b) Prove that for slow input phase variations the output tracks the input. (2 p)

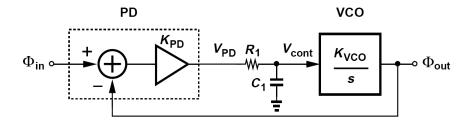
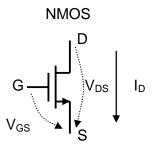
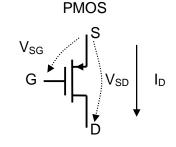


Fig. 5. Block level description of a PLL.

Page 6(6)

### **TRANSISTOR EQUATIONS**





#### **NMOS**

 $I_{\rm D} = 0 \qquad (V_{\rm GS} < V_{\rm TN})$  $\frac{V_{\rm DS}^2}{2} \qquad (V_{\rm GS} > V_{\rm TN})$ **Cutoff:** •

Linear mode:  

$$I_D = \mu_n C_{ox} \frac{W}{L} \left( (V_{GS} - V_{TN}) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

$$V_{GS} > V_{TN}$$
) and  $(V_{DS} < V_{GS} - V_{TN})$ 

Saturation mode: •

$$I_{D} = \frac{1}{2} \mu_{n} C_{ox} \frac{W}{L} (V_{GS} - V_{TN})^{2} (1 + \lambda V_{DS}) \qquad (V_{GS} > V_{TN}) \text{ and } (V_{DS} > V_{GS} - V_{TN})$$

• **On-resistance in triode region:**  $R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TN})}$ 

### **PMOS**

- $I_D = 0 \qquad (V_{GS} < |V_{TP}|)$ **Cutoff:** •
- Linear mode: ٠

$$I_{D} = \mu_{p} C_{ox} \frac{W}{L} \left( \left( V_{SG} - |V_{TP}| \right) V_{SD} - \frac{V_{SD}^{2}}{2} \right) \qquad (V_{GS} > |V_{TP}|) \text{ and } (V_{SD} < V_{SG} - |V_{TP}|)$$

Saturation mode: ٠

$$I_{D} = \frac{1}{2} \mu_{p} C_{ox} \frac{W}{L} (V_{SG} - |V_{TP}|)^{2} (1 + \lambda V_{SD}) \qquad (V_{GS} > |V_{TP}|) \text{ and } (V_{SD} > V_{SG} - |V_{TP}|)$$

• On-resistance in triode region: 
$$R_{on} = \frac{1}{\mu_p C_{ox} \frac{W}{L} (V_{SG} - |V_{TP}|)}$$