TSEK03: Radio Frequency Integrated Circuits (RFIC)

Lecture 10: PLL

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Overview

- Razavi: Chapter 9, pp. 609-639.
  - **9.1 Basic Concepts**
  - 9.2 Type-I PLLs
  - 9.3 Type-II PLLs
- Razavi: Chapter 10 highlights (from 10.1-10.3)
- Razavi: Chapter 11 highlights (from 11.1-11.2)

- Lee: Chapter 16.

Phase-Locked Loops

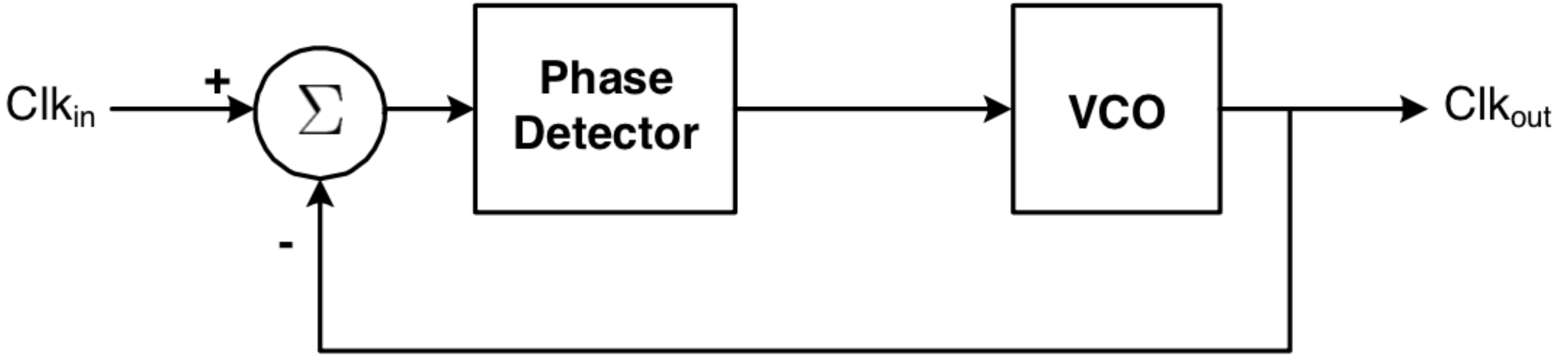
- Phase-locked loops (PLLs) are key components in many communication systems.
- They can generate an output signal whose frequency is a multiple of a fixed input frequency.
- PLLs can be involved in many applications such as:
  - Modulation and demodulation
  - Skew compensation
  - Data and clock recovery
  - Clock signal generation
- PLLs consist of a feedback system and they are typically higher-order systems. Stability concerns are very crucial.

Historical background (Lee)

- First described by Bellescize (1932) for AM demodulation with a homodyne receiver (IF=0). A frequency and phase stable LO (affects gain) is needed => LO with phase-locking.
- TV-receivers needs to synchronize the sweeps with the original signal to achieve a stable picture.
  - Early receivers used a simplified solution, injection-locking, to achieve this. A free-running oscillator, with lower frequency than the transmitted sweep and its synchronization signals, was used with a sawtooth oscillator to provide the synchronization. However, the oscillator needed manual course tuning, otherwise picture scrolling appeared. Also, it did not work well with noise.
- Today, TV-sets are using integrated PLLs => problem has disappeared.

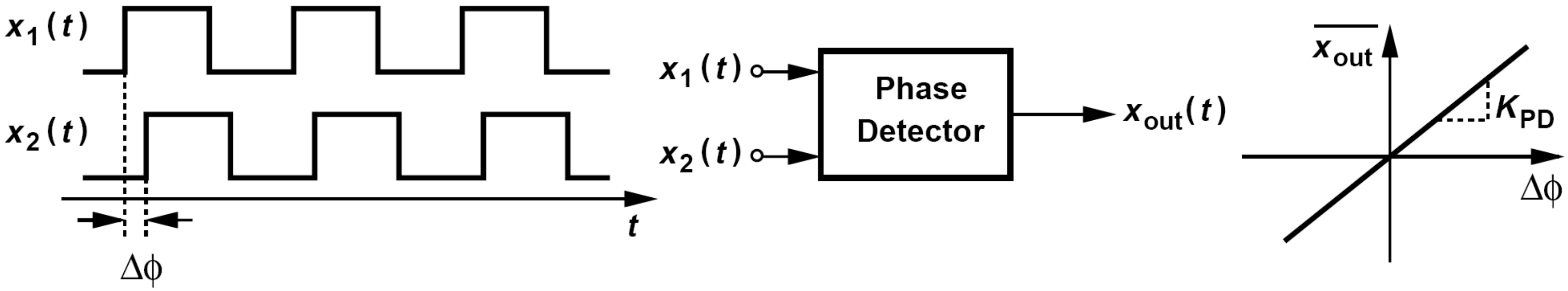
PLL: the principle

- General idea: Phase detector drives the VCO frequency so that the phase difference is reduced.
- A negative feedback system.
- Phase can be 0° but also commonly 90°.
- When lock has been achieved, we generally assume linear behavior of the blocks.



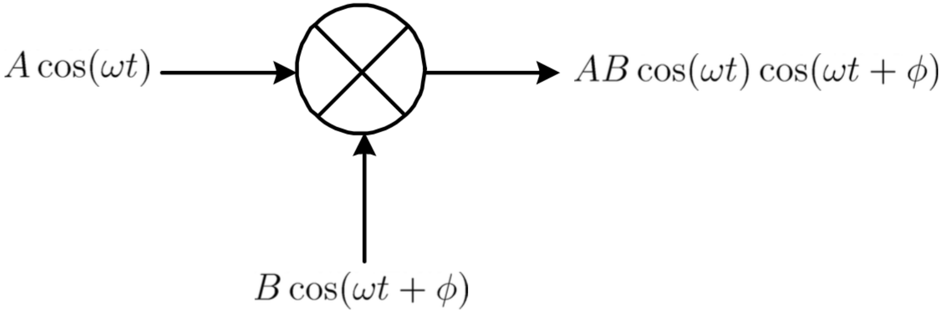
Phase Detector (PD)

- A Phase Detector (PD) is a circuit that senses two periodic inputs and produces an output whose *average* value is proportional to the difference between the *phases* of the inputs
- The input/output characteristic of the PD is ideally a straight line, with a slope called the "gain" and denoted by K_{PD} [V/rad].



PD: analog signals

- A multiplier (mixer) can operate as a phase detector.



$$AB\cos(\omega t)\cos(\omega t+\phi) = \frac{AB}{2}[\cos\phi - \cos(2\omega t+\phi)]$$

- We are interested in the DC value:

$$\langle AB\cos(\omega t)\cos(\omega t+\phi)\rangle = \frac{AB}{2}\cos\phi$$

PD: analog signals

- The gain of this phase detector is defined by

$$K_D = \frac{d}{d\phi} \langle V_{out} \rangle = -\frac{AB}{2} \sin\phi$$

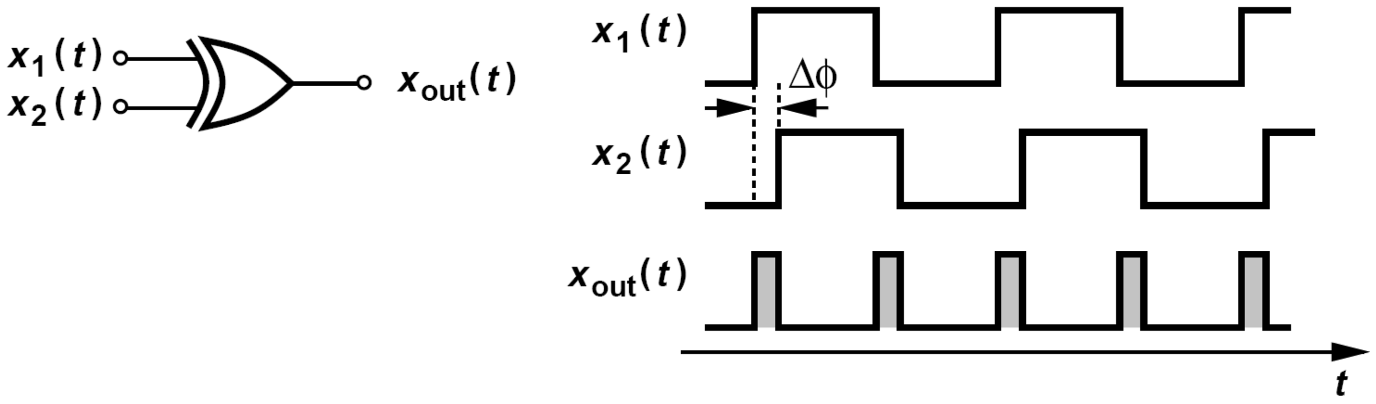
- This gain is maximum for ϕ = 90°. Then loop should be arrange to lock when ϕ = 90°. For this reason a multiplier is often called a quadrature phase detector.
- Although the phase difference is 90°, in an ideal quadrature loop we calculate the deviation from the equilibrium condition of 90°, and there the *phase error* is defined as zero.

PD: square wave signals

- What happens if we feed the multiplier with square waves?
- Expressions are quite similar to those presented for a sinusoidal case, but as square waves have harmonics, the feedback loop might lock to one of the harmonics instead of the fundamental (may also be wanted in some designs).
- If it is not desired, VCO range should be limited to avoid this kind of locking.
- Since harmonics are dropping with 1/f, locking to higher harmonics is not as easy as locking to the fundamental one.

PD: square wave signals

- Since in a square wave, signal is periodically inverting, we can use switches (specially in CMOS technology) to implement multiplier.
- We seek a circuit whose average output is proportional to the input phase difference.
- An Exclusive-OR (XOR) gate can serve this purpose. It generates pulses whose width are equal to Δϕ.
- The average output signal is a function of the phase difference.



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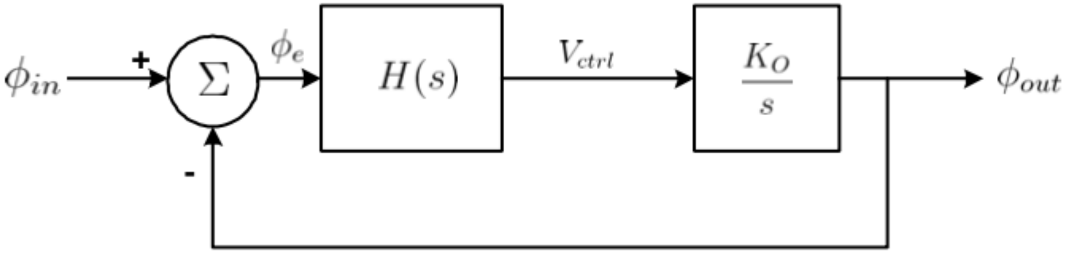
PLLs

- PLLs are traditionally classified as:
  - PLL type I, or first-order PLL:
    H(s) is a constant value amplifier, one pole (VCO).
  - PLL type II, or second-order PLL:
    H(s) contains poles, e.g. an integrator.



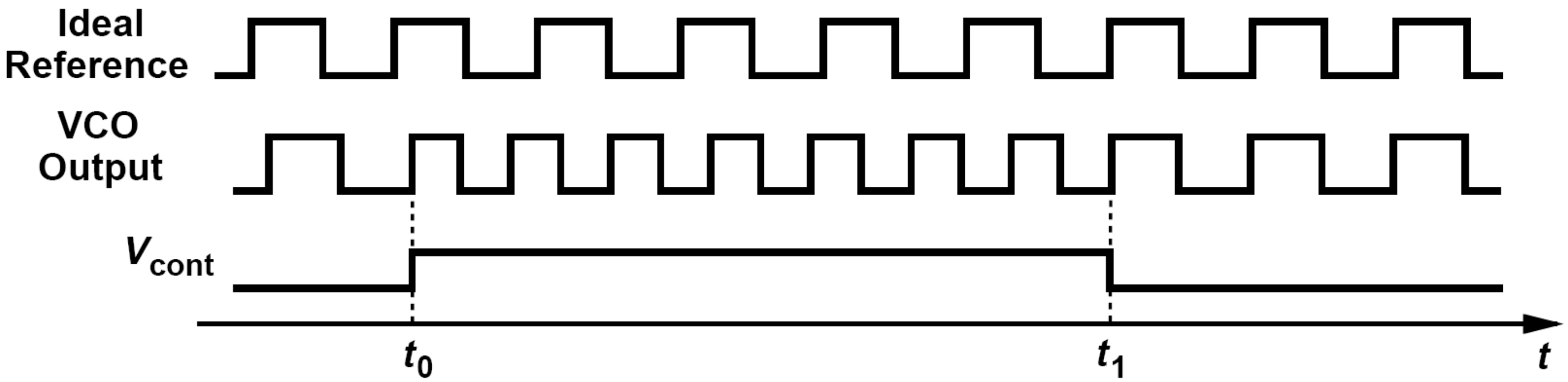
9.2 Type-I PLL: phase alignment

- Oscillation is at same frequency but with phase error.
- To null the finite phase error, we must:

(1) change the frequency of the VCO,

(2) allow the VCO to accumulate phase so that the phase error vanishes,

(3) change the frequency back to its initial value.

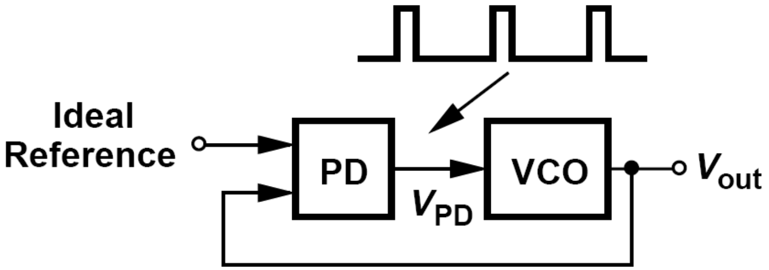


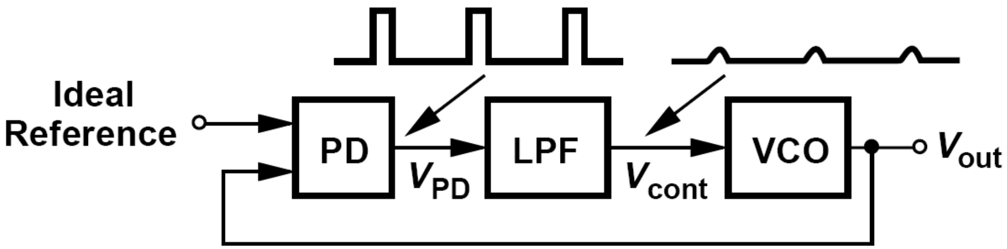
Type-I PLL: architecture and loop filter

- Negative feedback loop: if the “loop gain” is sufficiently high, the circuit minimizes the input error.
- The PD produces repetitive pulses at its output, modulating the VCO frequency and generating large sidebands:

$$V_{out} = A\cos\left[\omega_0 t + K_{VCO}\int V_{cont}dt\right]$$

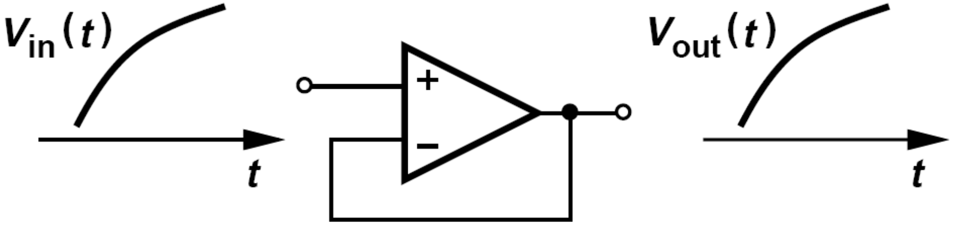
- Interpose a low-pass filter between the PD and the VCO to suppress these pulses.

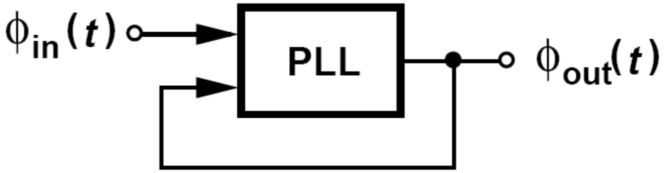




9.2.2 Type-I PLL: locking

- We say the loop is "locked" if *$\Phi_{out}(t)$- $\Phi_{in}(t)$* is constant with time.
- An important and unique consequence of phase locking is that the input and output frequencies of the PLL are exactly equal.



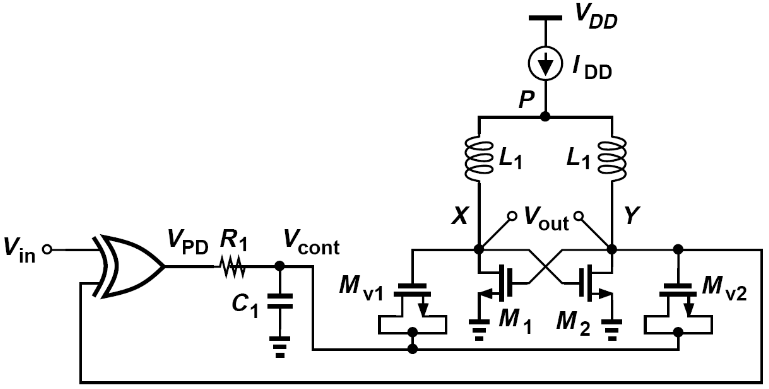


$$\phi_{out}(t) - \phi_{in}(t) = \text{constant}$$

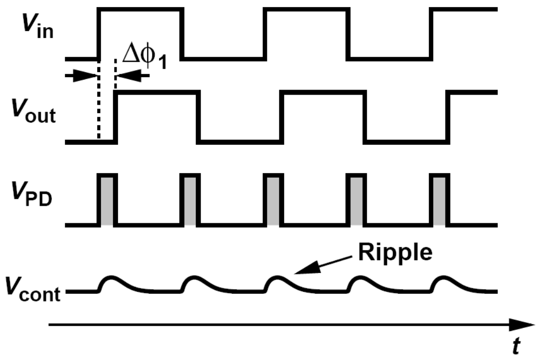
$$\frac{d\phi_{out}}{dt} = \frac{d\phi_{in}}{dt}$$

9.2.3 Type-I PLL: analysis

- If the loop is locked, the input and output frequencies are equal, the PD generates repetitive pulses, the loop filter extracts the average level, and the VCO senses this level so as to operate at required frequency.



(a)



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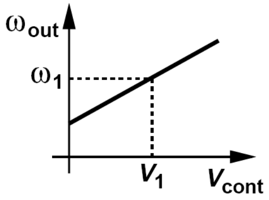
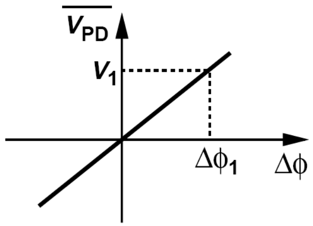


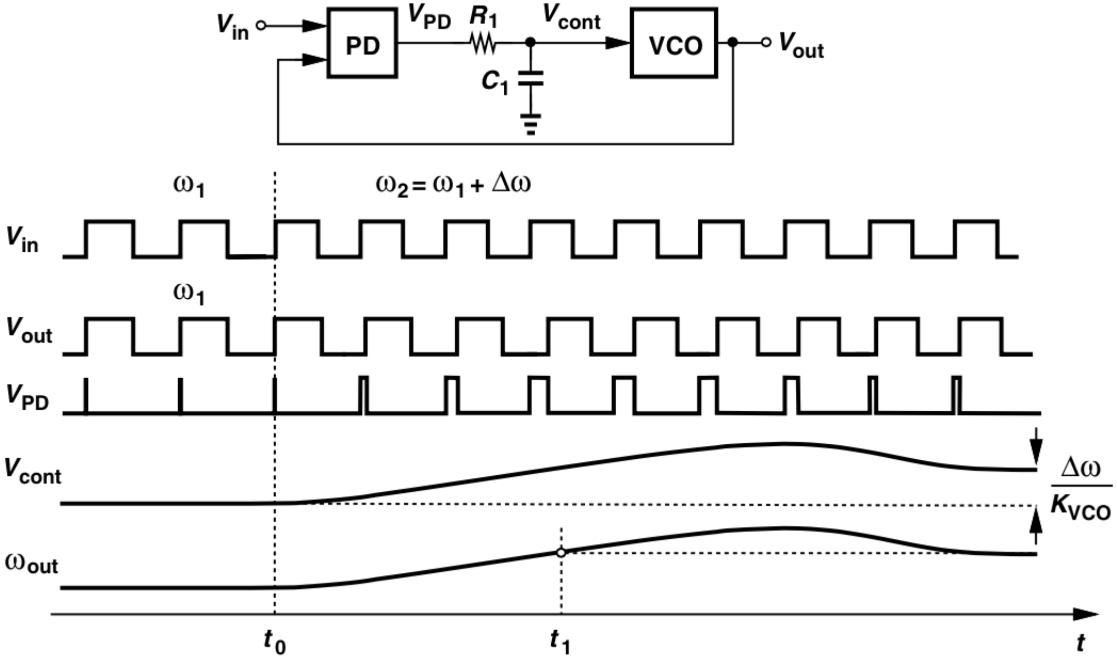


Type-I PLL: input frequency step

- The loop locks only after two conditions are satisfied:

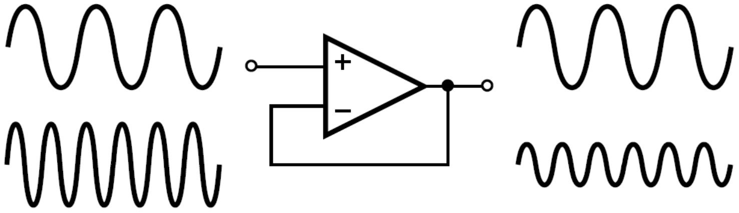
(1) ω_{out} becomes equal to ω_{in}

(2) the difference between ϕ_{in} and ϕ_{out} settles to its proper value



9.2.4 Loop Dynamics

- The transfer function of a voltage-domain circuit describes how a sinusoidal input <u>voltage</u> propagates to the output.
- The transfer function of a PLL reveals how a slow or a fast change in the input <u>phase</u> propagates to the output.



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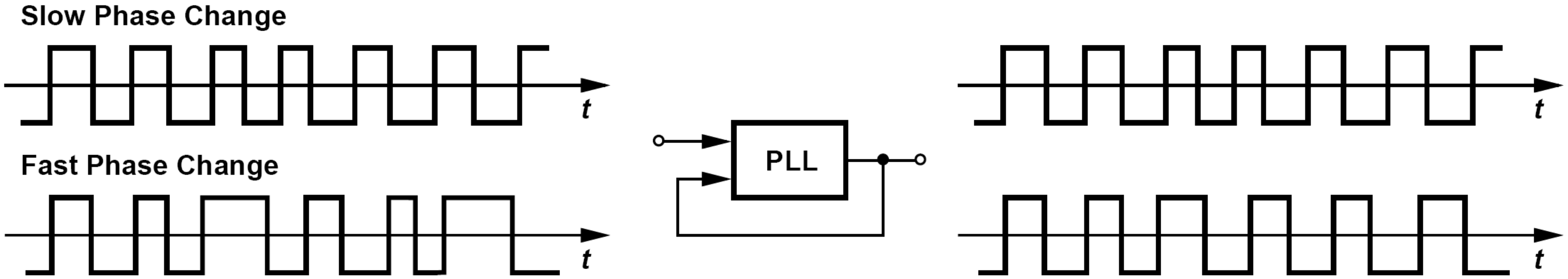
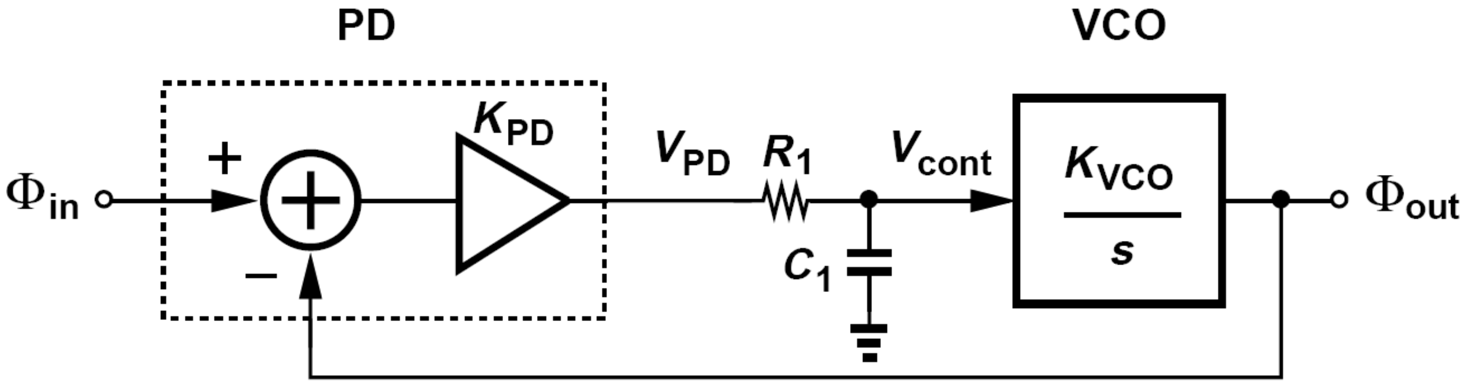


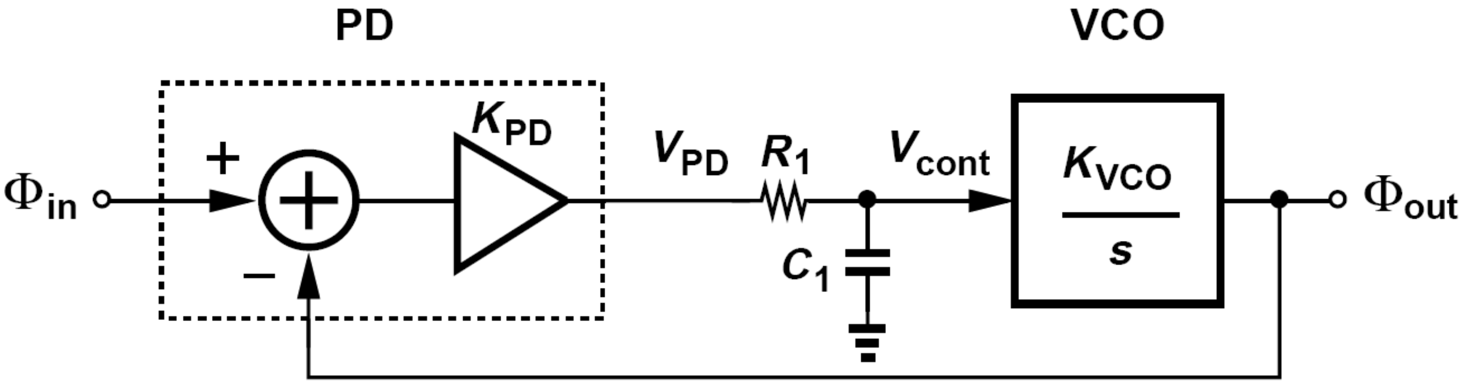
Phase domain model



- Open loop transfer function $[K_{PD}/(R_1C_1s+1)](K_{VCO}/s)$
- Overall closed-loop transfer function

$$H(s) = \frac{\phi_{out}}{\phi_{in}}(s) = \frac{K_{PD}K_{VCO}}{R_1C_1s^2+s+K_{PD}K_{VCO}}.$$

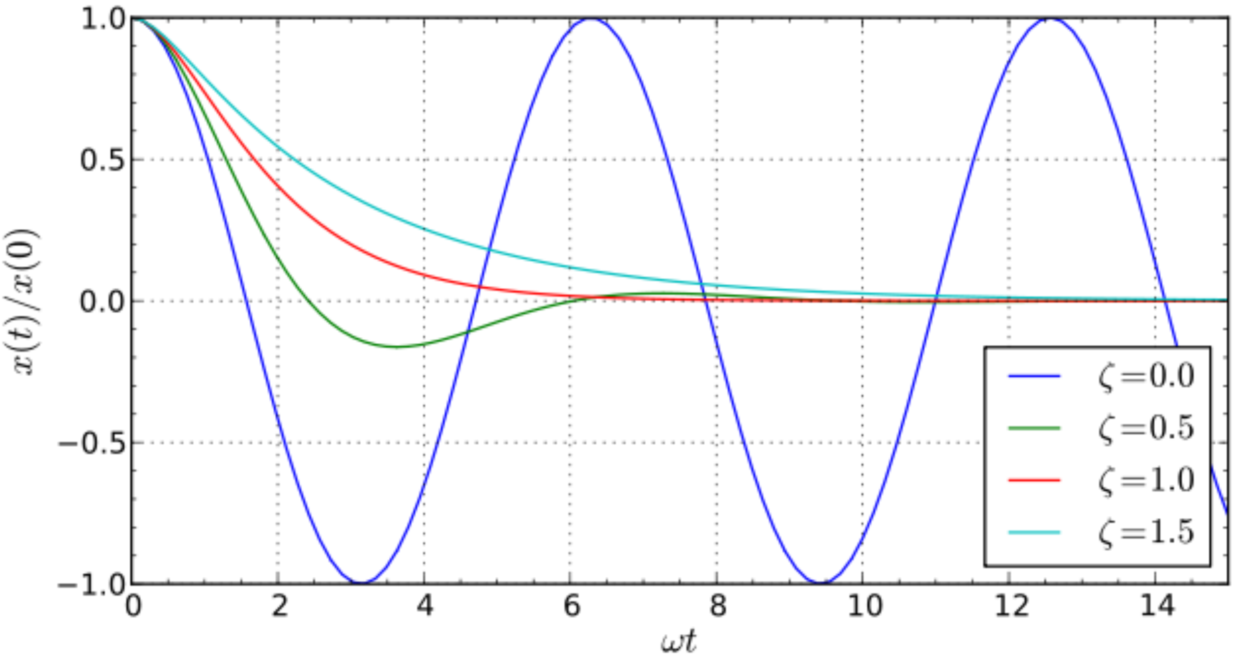
Phase domain model



- One pole at the origin (due to the VCO) => type-I PLL
- For slow input phase variation (s≈0), H(s)=1 and the output tracks the input phase.

Loop Dynamics - general

- Damping for phase changes:
  ζ=1 critically damped
  ζ<1 underdamped
  ζ>1 overdamped



Loop Dynamics

$$H(s) = \frac{\phi_{out}}{\phi_{in}}(s) = \frac{K_{PD}K_{VCO}}{R_1C_1s^2 + s + K_{PD}K_{VCO}}.$$

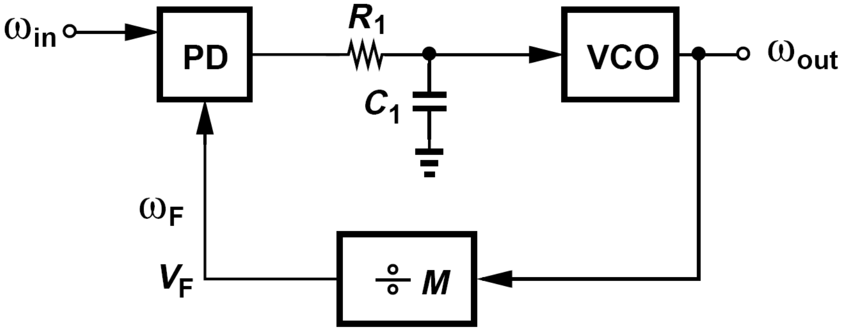
- We rewrite it as: $$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$
- where: $$\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD}K_{VCO}}}$$ damping factor or loop stability

$$\omega_n = \sqrt{K_{PD}K_{VCO}\omega_{LPF}}$$ natural frequency

- The damping factor ζ is typically chosen to be 1/√2 or larger so as to provide a well-behaved (critically damped or overdamped) response.

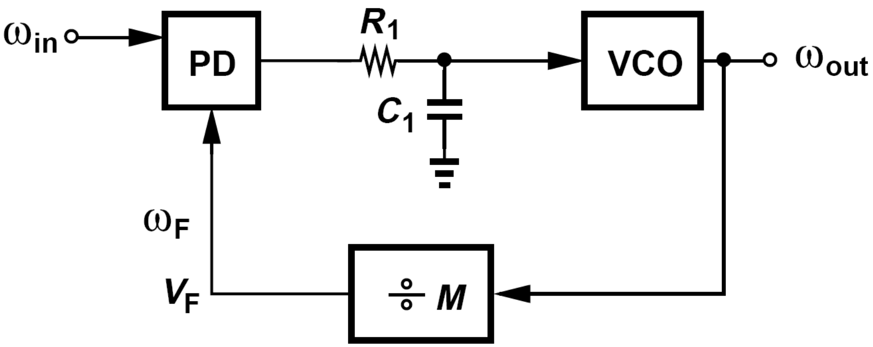
9.2.5 Frequency Multiplication

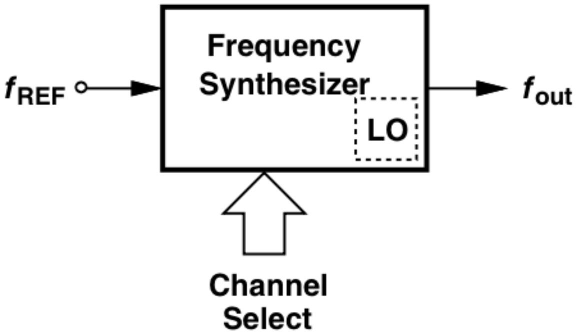
- Typically, oscillators with high quality factor do not provide wide tuning ranges.
- The output frequency of a PLL can be divided and then fed back.
- The ÷*M* circuit is a counter that generates one output pulse for every *M* input pulses.
- The divide ratio, *M*, is called the “modulus”.



Frequency Synthesizer

- If the divider modulus *M* changes by 1, the output frequency changes by ω_{in}.
- Can be used as frequency synthesizer (Ch 10).





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Type-II PLL

- Drawbacks with Type-I PLL:
  - Limited acquisition (locking) range. The PDs used in Type-I PLLs do not work when $\omega_1 <> \omega_2$.
  - Loop stability ζ tightly connected to the corner frequency of the low-pass filter, less stable loop.

1. we need to improve the PD to also detect frequency (widen the acquisition range)
=> Phase/Frequency Detector (PFD).

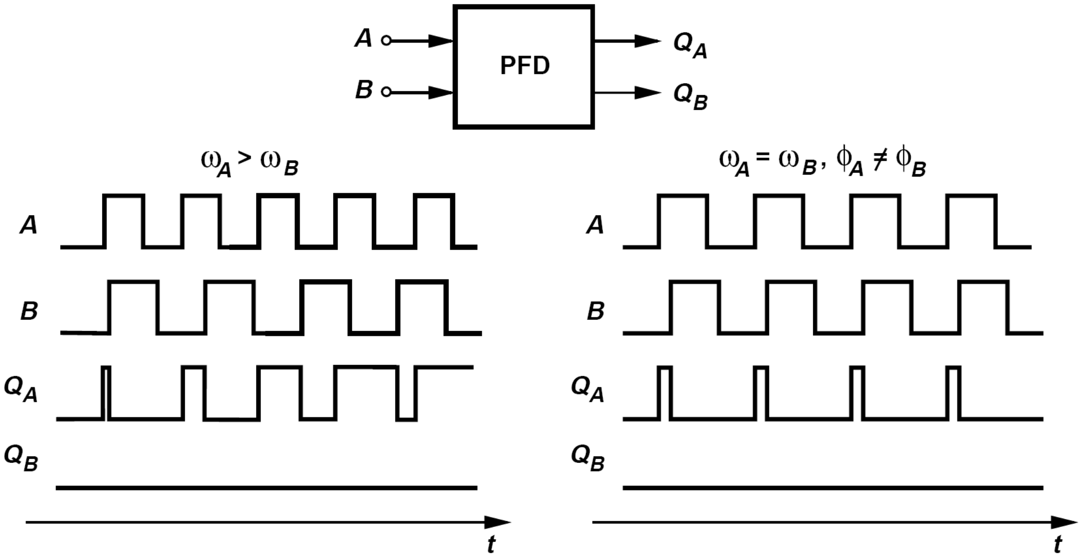
2. we also need to improve the trade-off between damping factor and corner frequency of the loop filter
=> Charge Pump (CP).

Phase/Frequency Detectors

- If the frequency of the VCO and the reference signal is not identical, the phase detector should be able to detect the frequency difference too.
- Multiplier-based or XOR-based phase detectors cannot provide this information.
- Sequential phase detectors can also be used to detect frequency. Main problem is their sensitivity to missing edges.
- Sequential phase detectors operate on edge transitions and they can provide a zero phase difference. Flip-flops are typically used as this kind of phase detectors.

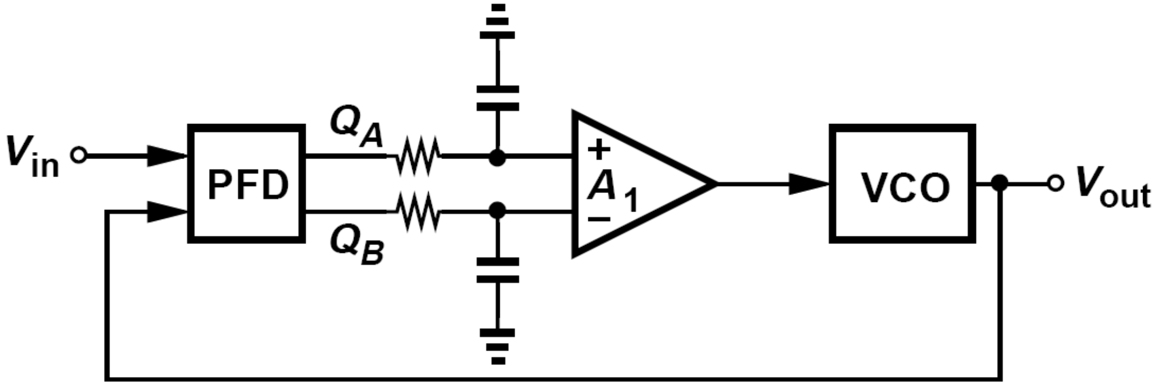
9.3.1 PFD for Type-II PLL

- Phase/Frequency Detector (PFD):
  - A rising edge on *A* yields a rising edge on Q_A (if Q_A is low)
  - A rising edge on *B* resets Q_A (if Q_A is high)
  - The circuit is symmetric with respect to *A* and *B* (and Q_A and Q_B)



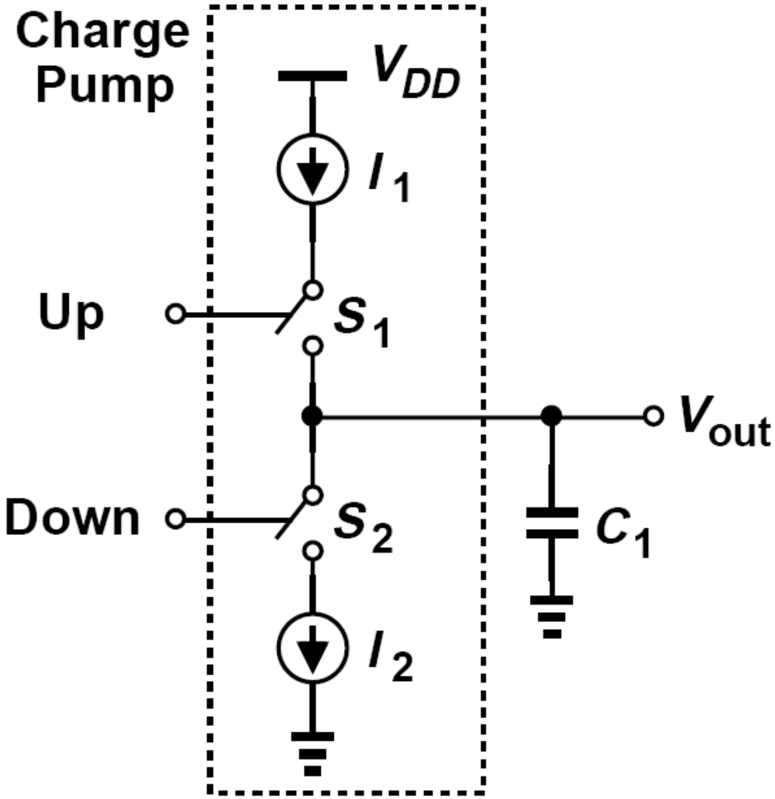
Use of PFD in a Type-I PLL

- Use of a PFD in a Type-I PLL resolves the issue of the limited acquisition range.
- At the beginning of a transient, the PFD acts as a frequency detector, pushing the VCO frequency toward the input frequency. After the two are sufficiently close, the PFD operates as a phase detector, bringing the loop into phase lock.



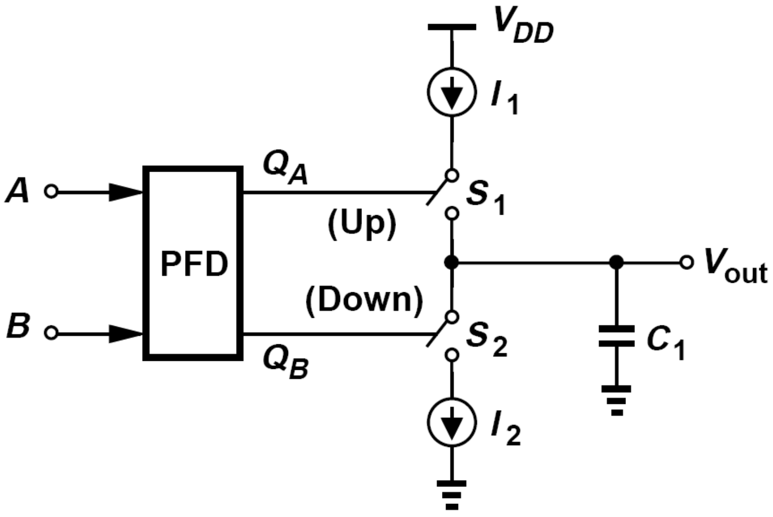
9.3.2 Charge Pump: overview

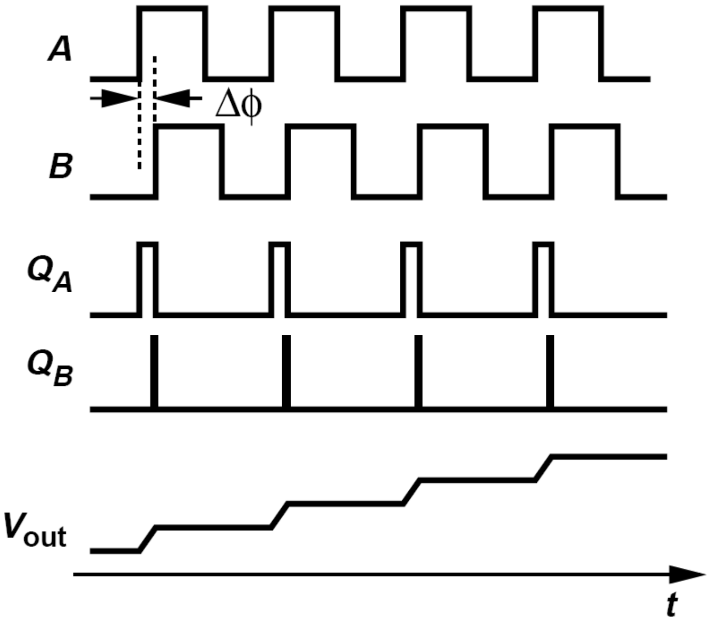
- Switches S_1 and S_2 are controlled by the inputs “Up” and “Down”, respectively.
- A pulse of width ΔT on Up turns S_1 on for ΔT seconds, allowing I_1 to charge C_1. V_{out} goes up by $\Delta T \cdot I_1/C_1$
- Similarly, a pulse on Down yields a drop in V_{out}.
- If Up and Down are asserted simultaneously, I_1 simply flows through S_1 and S_2 to I_2, creating no change in V_{out}.



Operation of the PFD/CP cascade

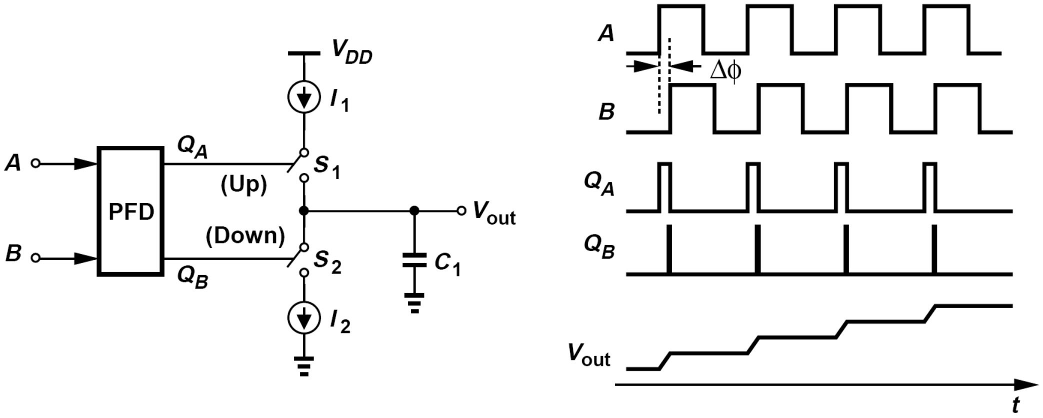
- An arbitrarily small (constant) phase difference between *A* and *B* still turns one switch on, thereby charging or discharging C_1 and driving V_{out} toward +∞ or -∞

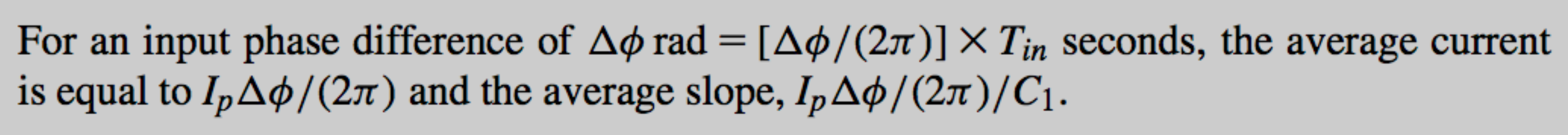




Example 9.14

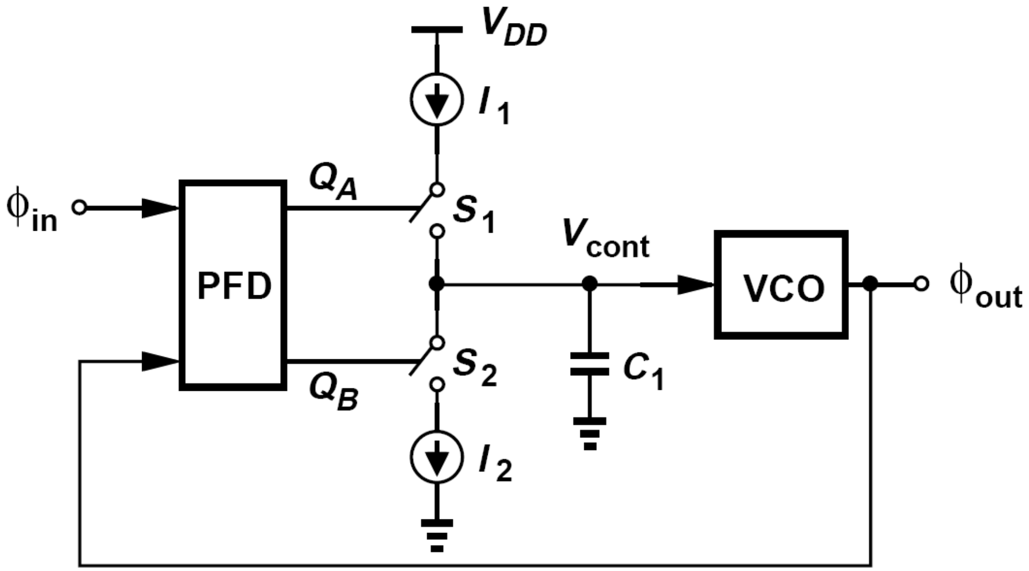
- We can approximate the PFD/CP circuit of figure below as a current source of some average value driving C_1. Calculate the average value of the current source and the output slope for an input period of T_{in}.




For an input phase difference of $\Delta\phi$ rad $= [\Delta\phi/(2\pi)] \times T_{in}$ seconds, the average current is equal to $I_p\Delta\phi/(2\pi)$ and the average slope, $I_p\Delta\phi/(2\pi)/C_1$.

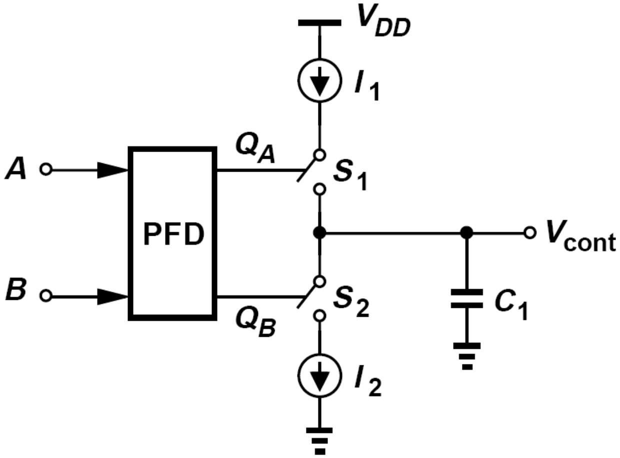
9.3.3 Charge-Pump PLLs: first attempt

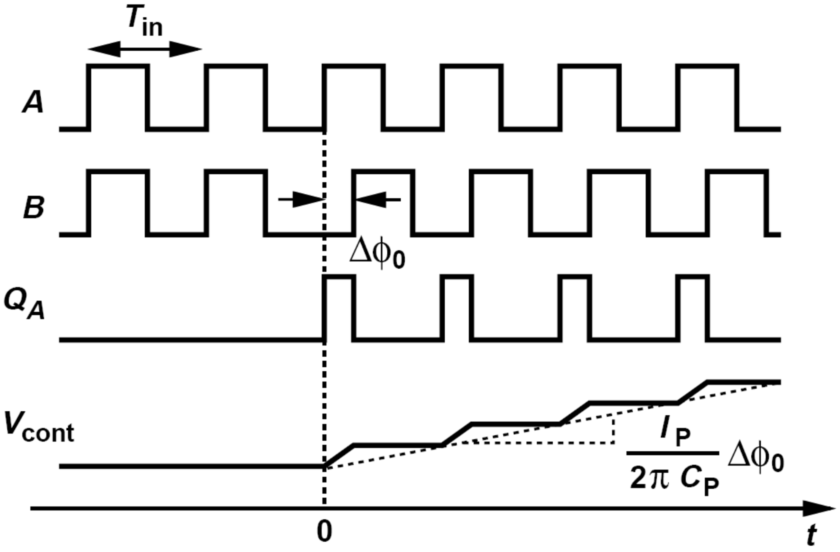
- When a CP is used in a PLL, the feedback loop ideally forces the input phase error to zero because a finite error would lead to an unbounded value for V_{cont}.



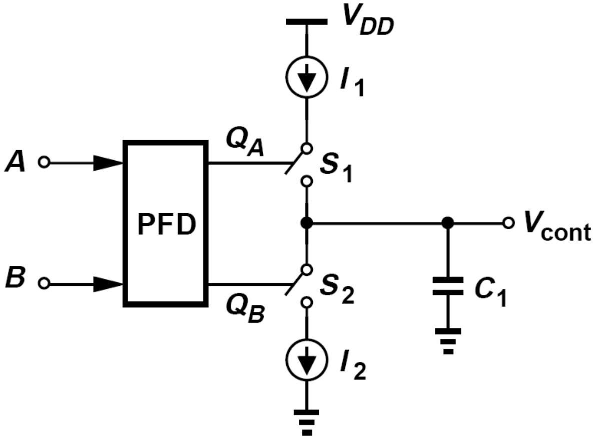
PFD/CP Transfer Function

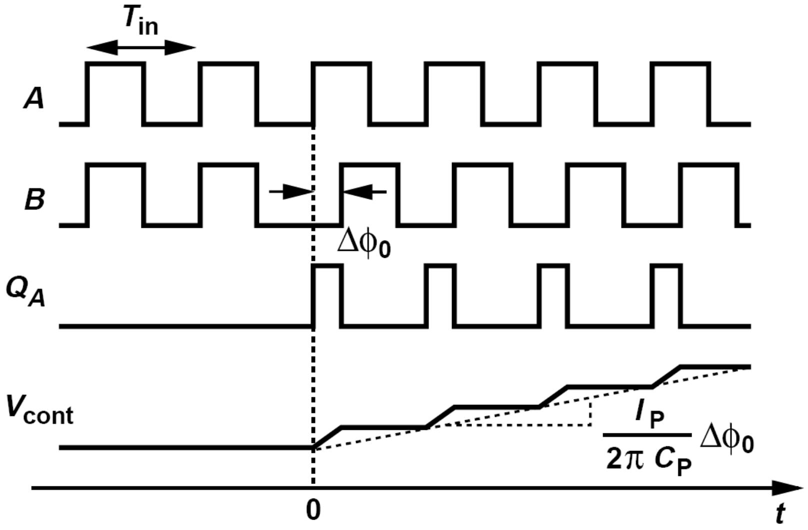
- $+\Delta\Phi$ => increased V_{out}.
- NB: But not all increases in $\Delta\Phi$ leads to increased V_{out}, so not linear for all/large $\Delta\Phi$.
- If approximated by a ramp, it is easier to analyze! "Continuous-time (CT)" approximation.





PFD/CP Transfer Function





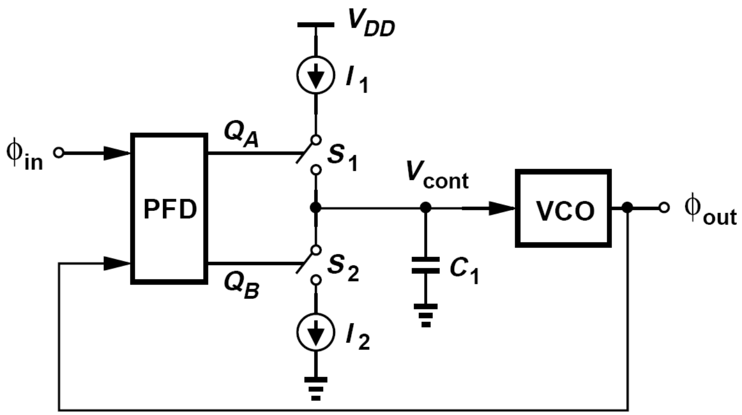
$$\Delta V_{cont} = \frac{\Delta\phi_0}{2\pi} T_{in} \frac{I_p}{C_1}$$

$$\frac{V_{cont}}{\Delta\phi}(s) = \frac{I_p}{2\pi C_1}\frac{1}{s}$$

$$V_{cont}(t) \approx \frac{\Delta\phi_0}{2\pi}\frac{I_p}{C_1} t u(t)$$

Charge-Pump PLLs: first attempt

- When a CP is used in a PLL, the feedback loop ideally forces the input phase error to zero because a finite error would lead to an unbounded value for V_{cont}.

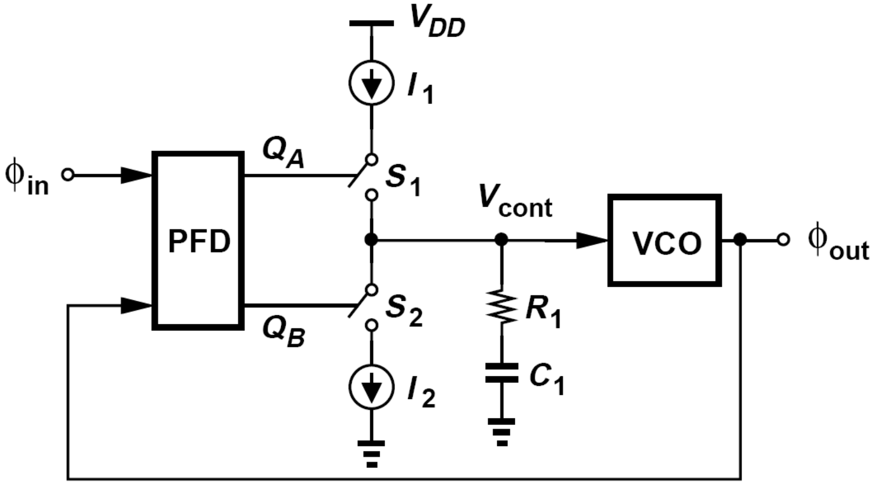


$$H(s) = \frac{\dfrac{I_p}{2\pi C_1 s} \cdot \dfrac{K_{VCO}}{s}}{1 + \dfrac{I_p}{2\pi C_1 s} \cdot \dfrac{K_{VCO}}{s}}$$

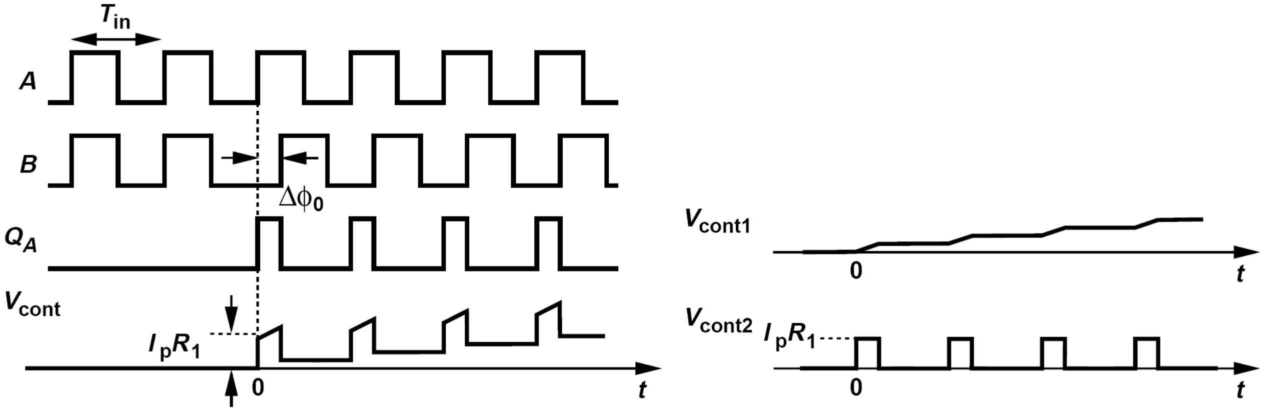
$$= \boxed{\frac{I_p K_{VCO}}{2\pi C_1 s^2 + I_p K_{VCO}}.}$$

Charge-Pump PLL

- Can oscillate! But make one of the integrators lossy, and the system is stabilized!
- This can be accomplished by inserting a resistor in series with C_1. The resulting circuit is called a “charge pump PLL” (CPPLL).



Transfer function



- Approximate the pulse sequence by a step of height $(I_pR_1)[\Delta\Phi_0/(2\pi)]$:

$$V_{cont}(t) = \frac{\Delta\phi_0}{2\pi}\frac{I_p}{C_1}tu(t) + \frac{\Delta\phi_0}{2\pi}I_pR_1u(t)$$

Transfer Function of CPPLL

- In the transfer function of PFD/CP, replacing *C_1* by series connection of *R_1* and *C_1* gives:

$$\frac{V_{cont}}{\Delta\phi}(s) = \frac{I_p}{2\pi}\left(\frac{1}{C_1 s} + R_1\right) \qquad (9.23)$$

- The closed-loop transfer function of this CPPLL is:

$$H(s) = \frac{\frac{I_p K_{VCO}}{2\pi C_1}(R_1 C_1 s + 1)}{s^2 + \frac{I_p}{2\pi} K_{VCO} R_1 s + \frac{I_p}{2\pi C_1} K_{VCO}}$$

Charge-Pump PLL

- Write the denominator as $s^2 + 2\zeta\omega_n s + \omega_n^2$

$$\begin{aligned} \zeta &= \frac{R_1}{2}\sqrt{\frac{I_p C_1 K_{VCO}}{2\pi}} \\ \omega_n &= \sqrt{\frac{I_p K_{VCO}}{2\pi C_1}}. \end{aligned}$$

- As ω_n decreases, C_1 increases, so does ζ (opposite of type-I PLL)
- Trade-off between stability and ripple amplitude is thus removed.

Type-I PLL

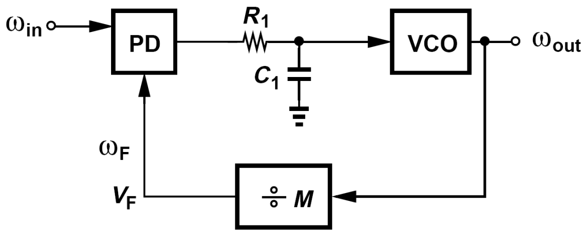
$$H(s) = \frac{\phi_{out}}{\phi_{in}}(s) = \frac{K_{PD}K_{VCO}}{R_1C_1s^2 + s + K_{PD}K_{VCO}}.$$

- We rewrite it as: $H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$
- where: $\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD}K_{VCO}}}$ damping factor or loop stability

$$\omega_n = \sqrt{K_{PD}K_{VCO}\omega_{LPF}}.$$

natural frequency

9.3.6 Frequency-Multiplying CPPLL



- Product of (9.23) and K_{VCO}/s as forward function, 1/M as feedback:

$$H(s) = \frac{\frac{I_p K_{VCO}}{2\pi C_1}(R_1 C_1 s + 1)}{s^2 + \frac{I_p}{2\pi}\frac{K_{VCO}}{M}R_1 s + \frac{I_p}{2\pi C_1}\frac{K_{VCO}}{M}}$$

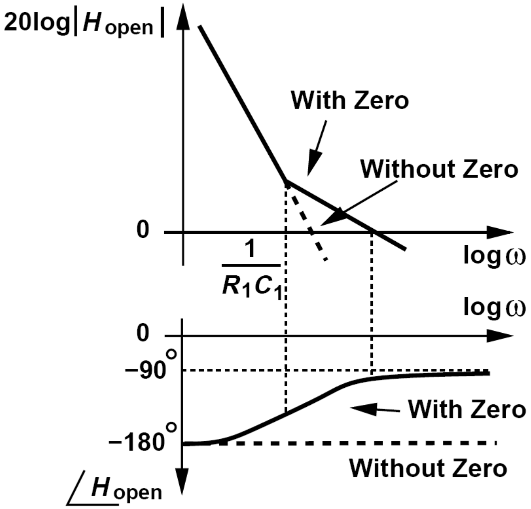
Frequency-Multiplying CPPLL

$$\zeta = \frac{R_1}{2}\sqrt{\frac{I_p C_1}{2\pi}\frac{K_{VCO}}{M}}$$

$$\omega_n = \sqrt{\frac{I_p}{2\pi C_1}\frac{K_{VCO}}{M}}.$$

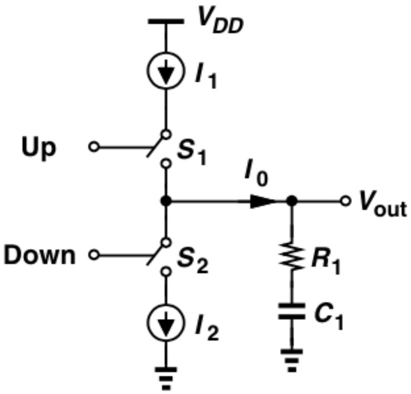
- As can be seen in the Bode plot, the division of K_{VCO} by M makes the loop less stable, requiring that I_p and/or C_1 be larger. We can rewrite the equation on the previous page as

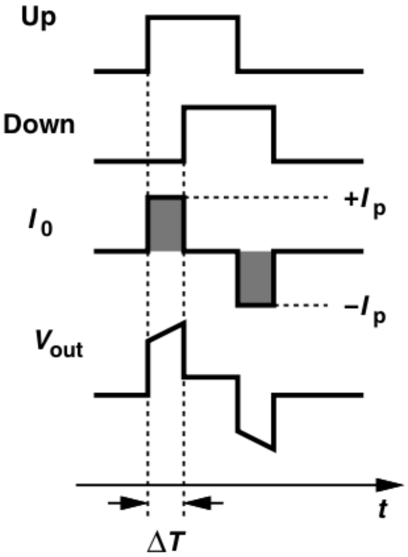
$$H(s) = M\frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$



Higher-Order Loops

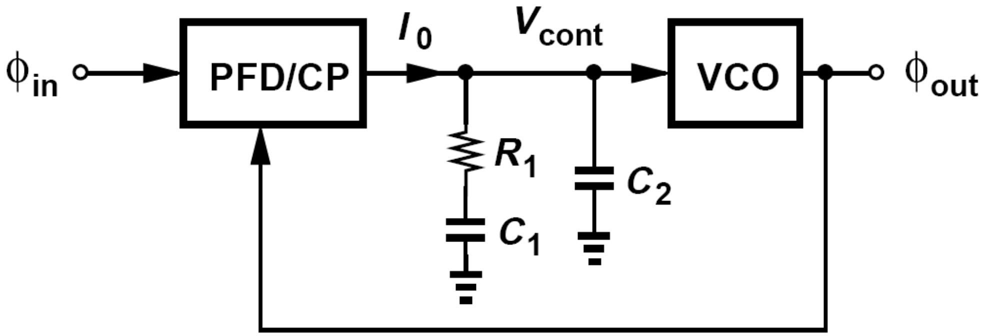
- The loop filter consisting of R_1 and C_1 may prove inadequate because, even in the locked condition, it does not suppress the ripple sufficiently.
- The ripple consists of positive ad negative pulses of amplitude I_pR_1 occurring every T_{in} seconds.

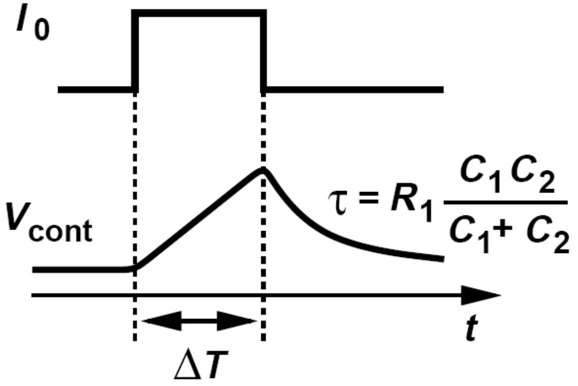




Higher-Order Loops

- Another capacitor C_2 can be added to suppress the ripple further.





- It increases the loop order and creates stability issues.
- Proper values should be chosen for R_1, C_1, and C_2, and careful calculation of phase margin is required.

Overview

- Razavi: Chapter 9, pp. 609-639.
  - 9.1 Basic Concepts
  - 9.2 Type-I PLLs
  - 9.3 Type-II PLLs
- **Razavi: Chapter 10 highlights (from 10.1-10.3**)
- Razavi: Chapter 11 highlights (from 11.1-11.2)

- Lee: Chapter 16.

Ch 10 Integer-N frequency synthesizers

- Example: Bluetooth = 2400 - 2480 MHz, 1 MHz channels.
- Free-running VC0 with PVT variations is not good enough as frequency generator.

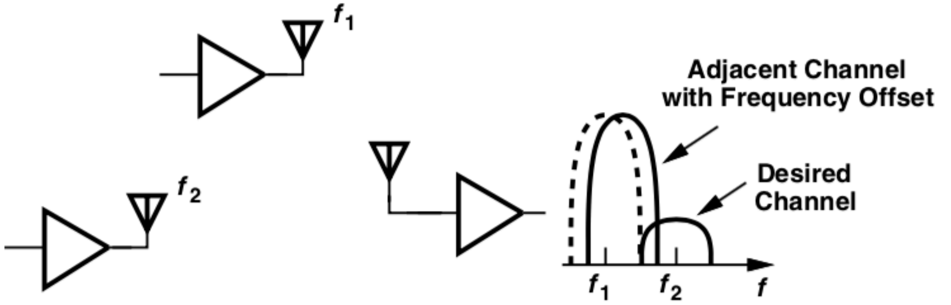
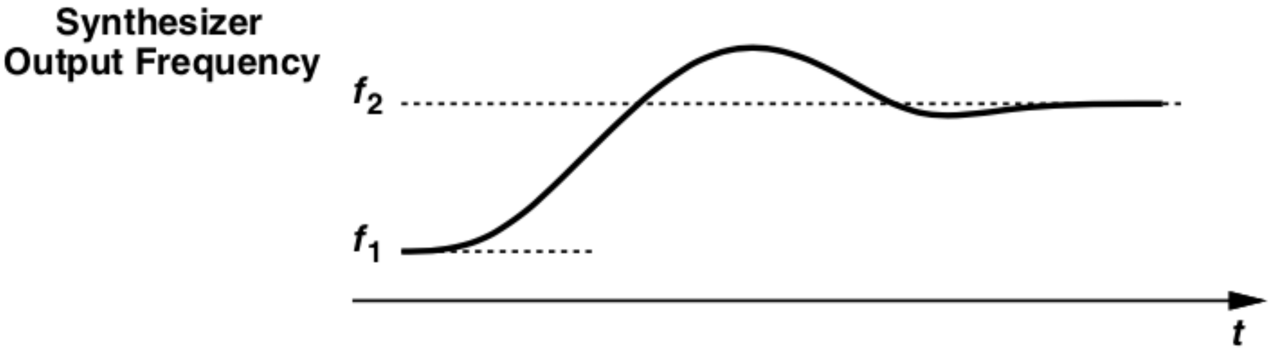


Figure 10.2 *Effect of LO frequency error in TX.*

- And other requirements: phase noise, sidebands, lock time

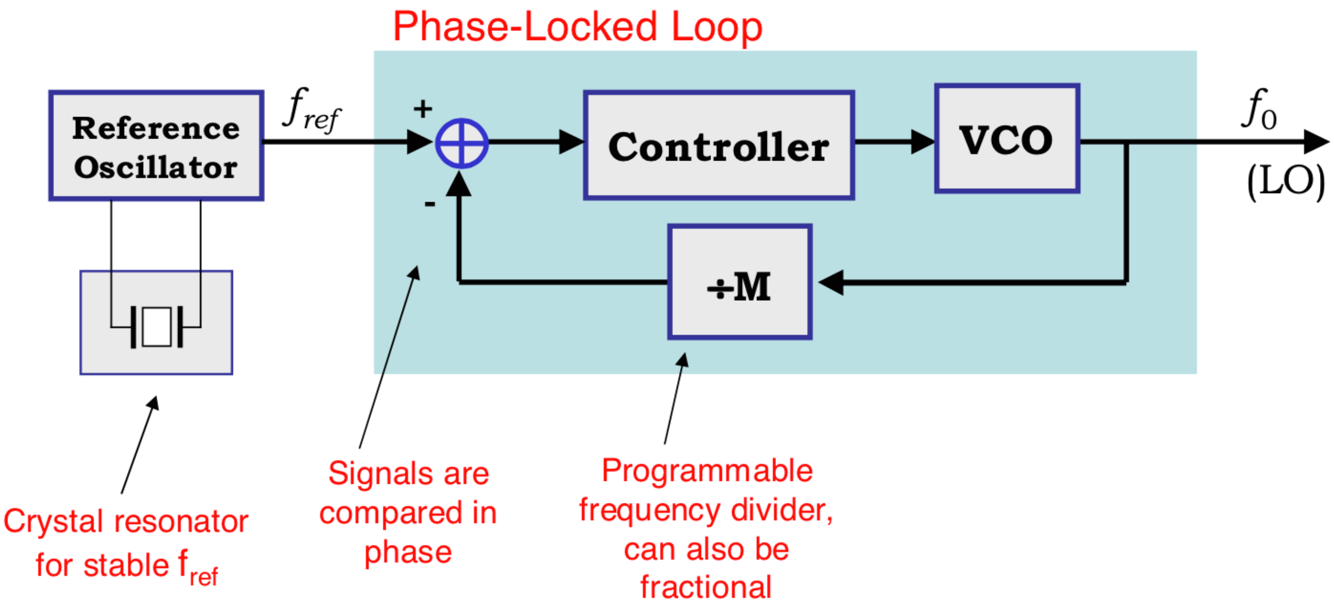
Lock time

- When the down-mixed channel is changed, the synthesizer takes a finite time to settle to a new output frequency.
- This is called “lock time” for synthesizers that employ PLLs.
- The settling time directly subtracts from the time available for communication.
- In typical RF systems, requirements vary from a few tens of milliseconds to a few tens of microseconds.



10.2 Basic Integer-N synthesizer

- Integer-N synthesizers: output frequency is an integer multiple of the reference frequency.
- If N increases by 1, then f_o increases by f_{REF} => the minimum channel spacing is equal to the reference frequency.



Crystal resonator for stable f_{ref}

Signals are compared in phase

Programmable frequency divider, can also be fractional

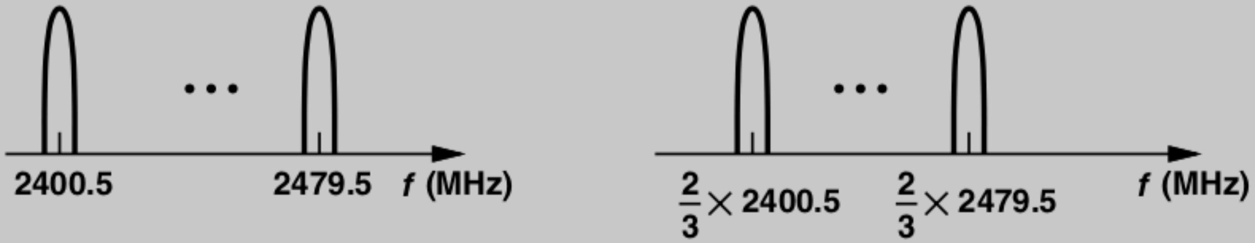
Example 10.3

Compute the required reference frequency and range of divide ratios for an integer-N synthesizer designed for a Bluetooth receiver. Consider two cases: (a) direct conversion, (b) sliding-IF downconversion with $f_{LO} = (2/3)f_{RF}$ (Chapter 4).

Solution:

(a) Shown in Fig. 10.10(a), the LO range extends from the *center* of the first channel, 2400.5 MHz, to that of the last, 2479.5 MHz. Thus, even though the channel spacing is 1 MHz, f_{REF} must be chosen equal to 500 kHz. Consequently, $N_1 = 4801$ and $N_2 = 4959$.

(b) As illustrated in Fig. 10.10(b), in this case the channel spacing and the center frequencies are multiplied by 2/3. Thus, $f_{REF} = 1/3$ MHz, $N_1 = 4801$, and $N_2 = 4959$.

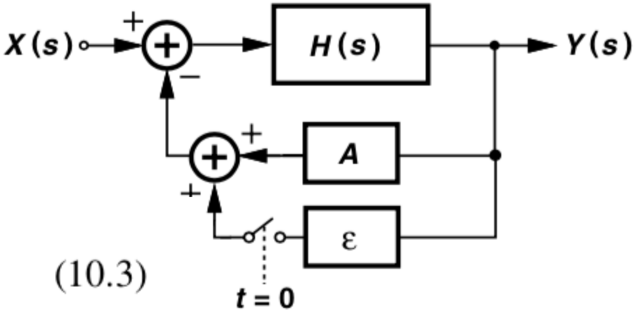


(a)

(b)

Figure 10.10 *Bluetooth LO frequency range for (a) direct and (b) sliding-IF downconversion.*

10.3 Settling behavior



- N changes at t=0:

$$Y(s) = \frac{H(s)}{1 + (A + \epsilon)H(s)} X(s) \qquad (10.3)$$

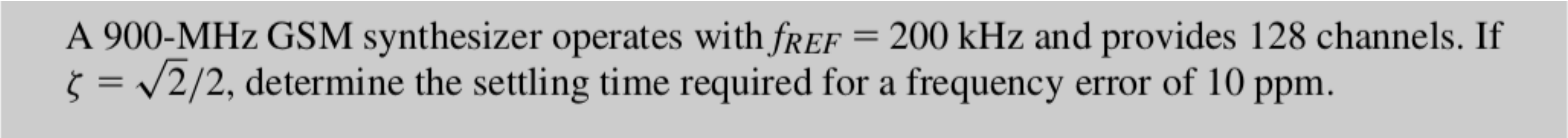
$$\approx \frac{H(s)}{1 + AH(s)} \cdot \frac{1}{1 + \epsilon/A} X(s) \qquad (10.4)$$

$$\approx \frac{H(s)}{1 + AH(s)} \left(1 - \frac{\epsilon}{A}\right) X(s), \qquad (10.5)$$

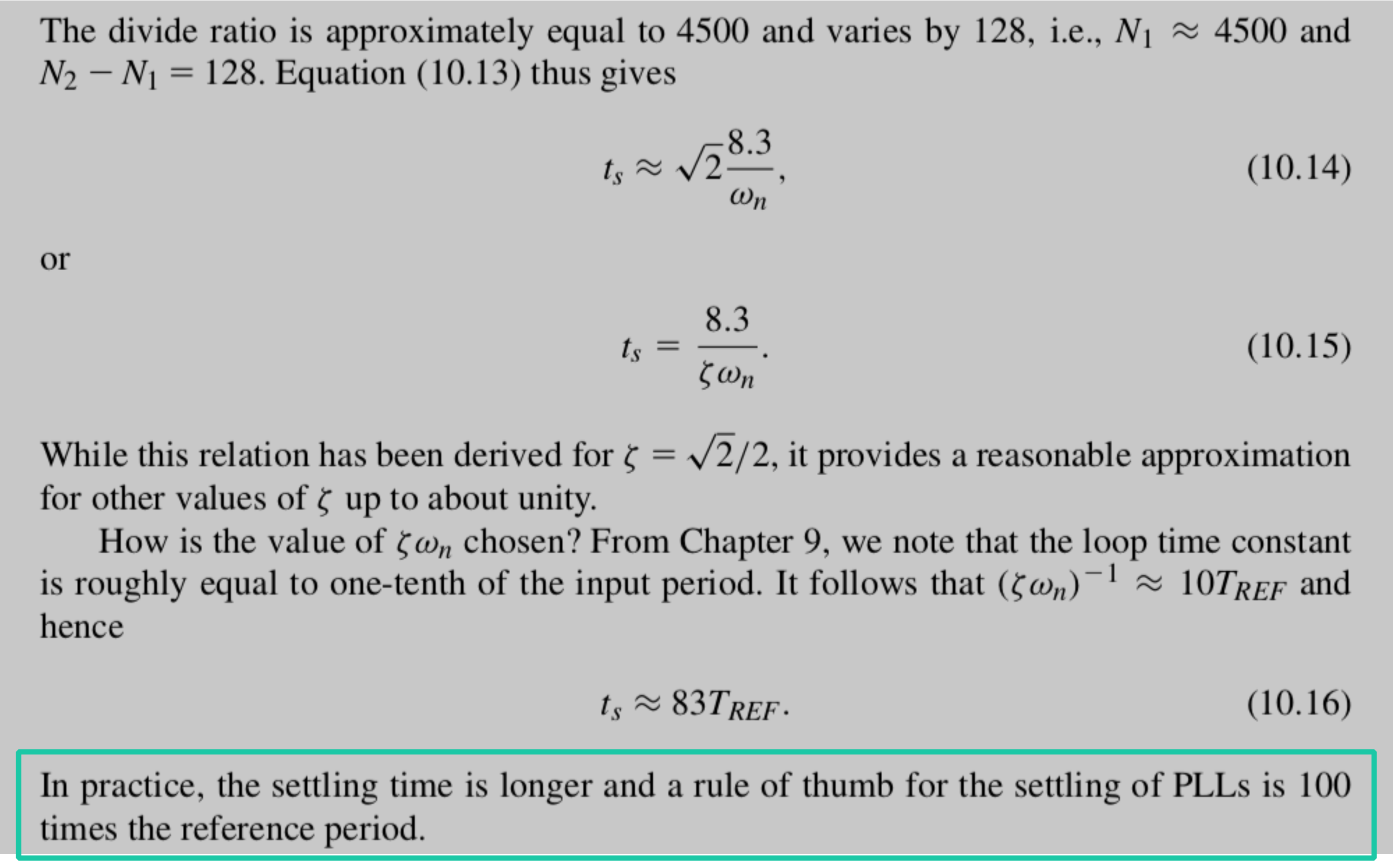
- Interpretation: a frequency jump of -(ε/A)f_0.
- When the divide ratio changes, the loop responds as if an input frequency step were applied, requiring a finite time to settle within an acceptable margin around its final value.
- Eq. 10.7 - 10.13 estimate the settling time (see book for details):

$$t_s = \frac{\sqrt{2}}{\omega_n} \ln \left| \sqrt{2} \left(1 - \frac{N_1}{N_2}\right) \frac{1}{\alpha} \right|. \qquad (10.13)$$

Example 10.5



A 900-MHz GSM synthesizer operates with $f_{REF} = 200$ kHz and provides 128 channels. If $\zeta = \sqrt{2}/2$, determine the settling time required for a frequency error of 10 ppm.



The divide ratio is approximately equal to 4500 and varies by 128, i.e., $N_1 \approx 4500$ and $N_2 - N_1 = 128$. Equation (10.13) thus gives

$$t_s \approx \sqrt{2}\frac{8.3}{\omega_n}, \tag{10.14}$$

or

$$t_s = \frac{8.3}{\zeta\omega_n}. \tag{10.15}$$

While this relation has been derived for $\zeta = \sqrt{2}/2$, it provides a reasonable approximation for other values of ζ up to about unity.

How is the value of $\zeta\omega_n$ chosen? From Chapter 9, we note that the loop time constant is roughly equal to one-tenth of the input period. It follows that $(\zeta\omega_n)^{-1} \approx 10T_{REF}$ and hence

$$t_s \approx 83T_{REF}. \tag{10.16}$$

In practice, the settling time is longer and a rule of thumb for the settling of PLLs is 100 times the reference period.

Overview

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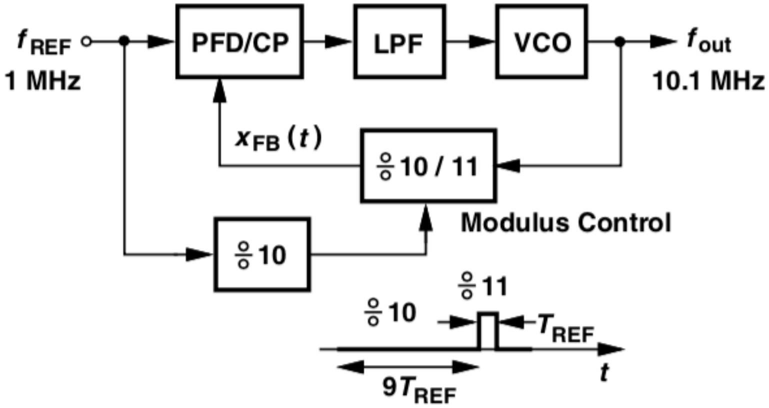
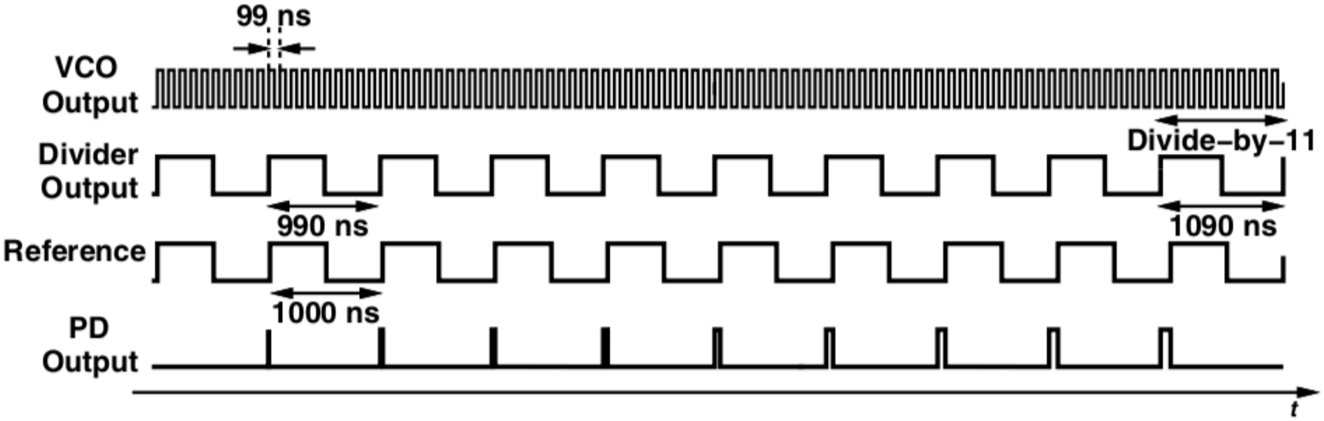
Ch 11 Fractional-N Synthesizers

- Wwhat happens if the divider divides by N for half of the time and by N+1 for the other half?
- The “average” modulus of the divider is now equal to [N + (N +1)]/2 = N + 0.5.
- If the PLL below divides by 10, 90% of the time, and 11, 10% of the time, f_{out} = 10.1 MHz.
- Arbitrary frequency steps can be provided with a fractional-n synthesizer!



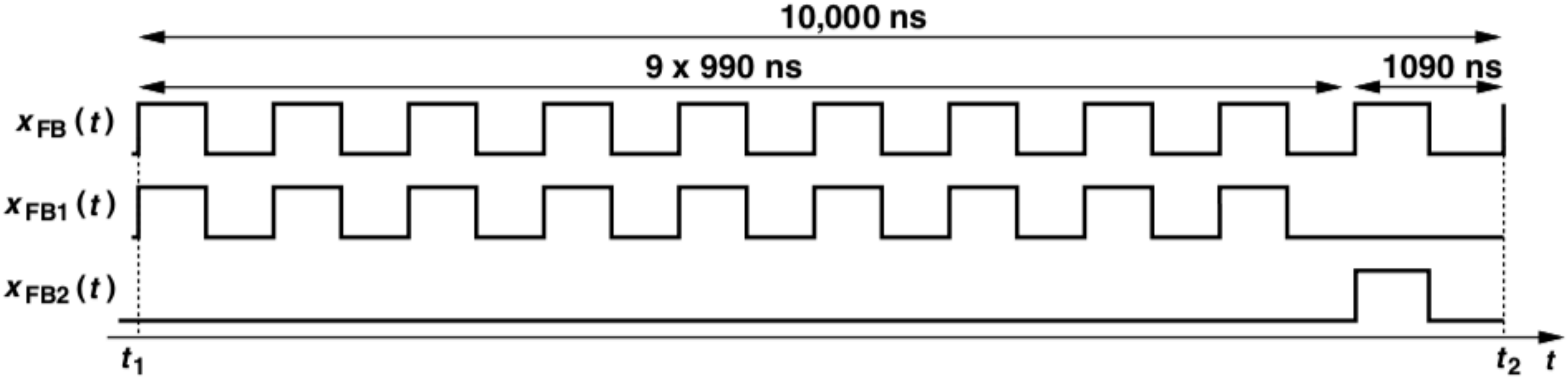
”Fractional spurs”

- Detailed view of the previous PLL. 990 ns pulse from the divider output (1/10.1 MHz = 99ns, * 10), and then 1000 ns for a short time (mult by 11)
- This creates a VCO modulation of 0.1 MHz + sidebands (0.1 MHz multiples), called fractional spurs.
- I.e., output frequency = (N + a)*$f_{REF,}$ spurs = 1(a*f_{REF}).

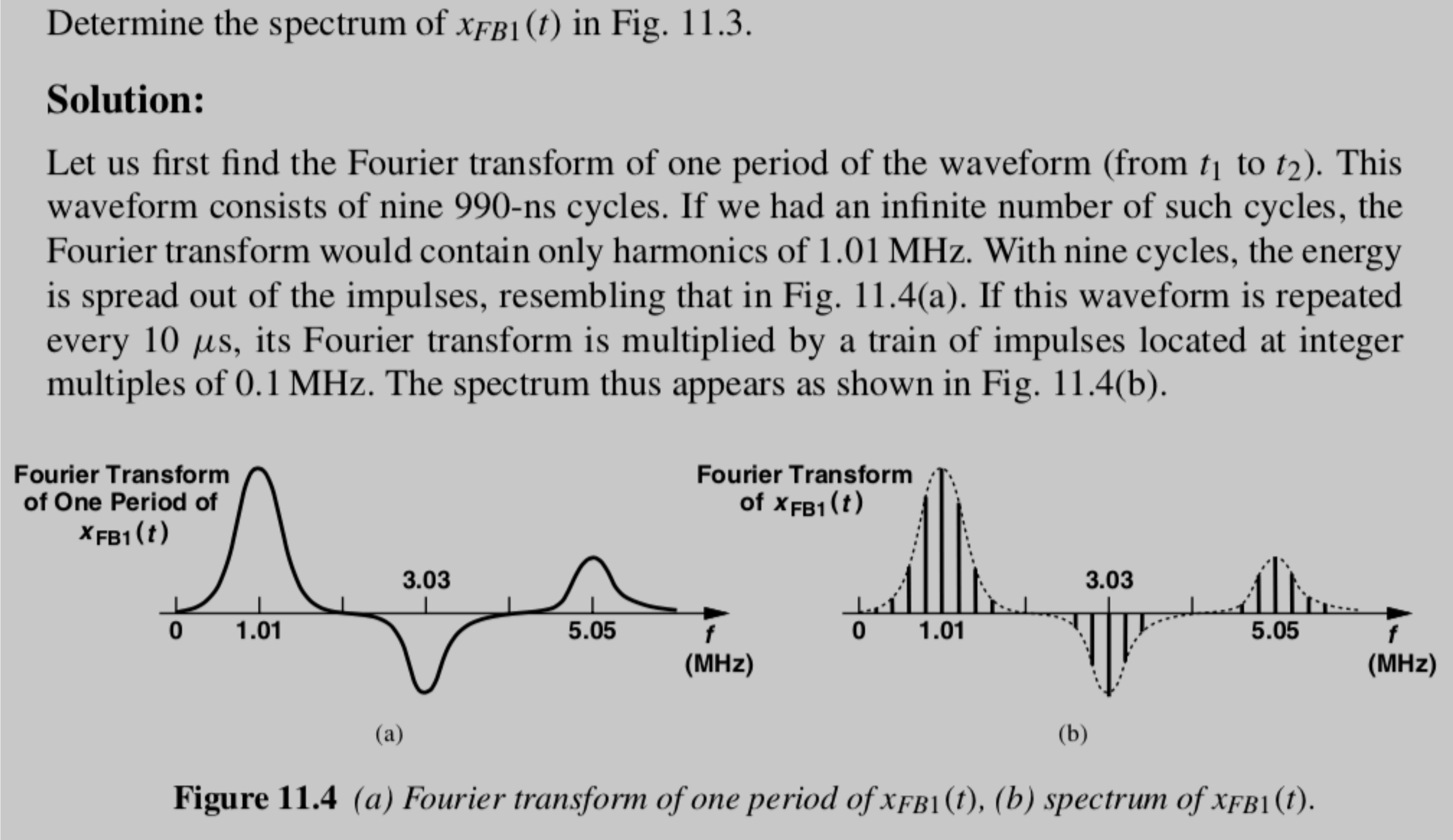


”Fractional spurs”

- The phase detector can be view as a mixer!
  - f_1 = 9 periods * 990 ns, ”dead time” 1090 ns, total 10 000 ns
  - f_2 = 1 period * 1090 ns.
- => harmonic at 0.1 MHz, 0.2 MHz, etc.



Example 11.1



Determine the spectrum of $x_{FB1}(t)$ in Fig. 11.3.

Solution:

Let us first find the Fourier transform of one period of the waveform (from t_1 to t_2). This waveform consists of nine 990-ns cycles. If we had an infinite number of such cycles, the Fourier transform would contain only harmonics of 1.01 MHz. With nine cycles, the energy is spread out of the impulses, resembling that in Fig. 11.4(a). If this waveform is repeated every 10 μs, its Fourier transform is multiplied by a train of impulses located at integer multiples of 0.1 MHz. The spectrum thus appears as shown in Fig. 11.4(b).

Fourier Transform of One Period of $x_{FB1}(t)$
3.03
0
1.01
5.05
f (MHz)
(a)
Fourier Transform of $x_{FB1}(t)$
3.03
0
1.01
5.05
f (MHz)
(b)

Figure 11.4 *(a) Fourier transform of one period of $x_{FB1}(t)$, (b) spectrum of $x_{FB1}(t)$.*

How to reduce fractional spurs (11.2)

- ”Hundreds of compensation techniques” (!).
- Modulus randomization: random toggling between the divisors, converts deterministic sidebands to noise.
- Noise shaping: minimizing the spectral density near the center frequency.

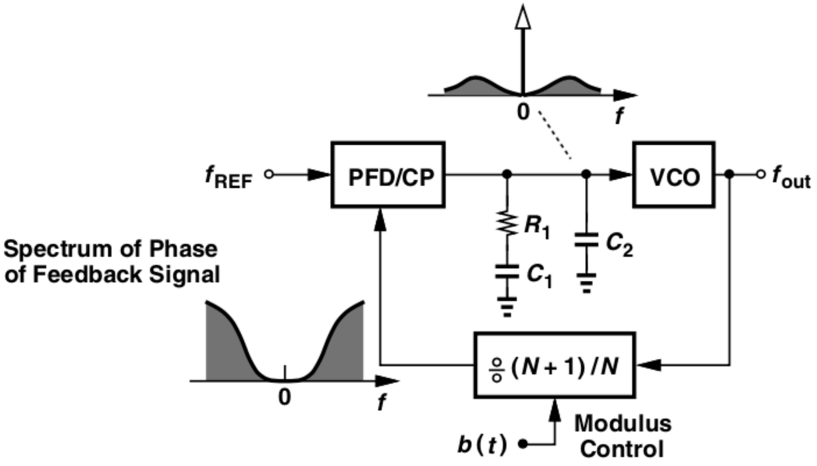


Figure 11.9 *Synthesizer employing modulus randomization.*