Written Test
TSEI30,
Analog and Discrete-time Integrated Circuits

Date	April 29, 2003
Time:	14 – 18
Place:	U14
Max. no of points:	70; 50 from written test, 5 for project, and 15 for assignments.
Grades:	30 for 3, 42 for 4, and 56 for 5.
Allowed material:	All types of calculators except Lap Tops. All types of tables and handbooks. The textbook Johns & Martin: Analog Integrated Circuit Design
Examiner:	Lars Wanhammar.
Responsible teacher:	Robert Hägglund. Tel.: 0705 - 48 56 88.
Correct (?) solutions:	Solutions and results will be displayed in House B, entrance 25 - 27, ground floor.

Good Luck!

Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

Solutions

1. Large-signal analysis

The circuit in the figure is a commonly used structure when designing analog circuits. In all following exercises assume that the transistor M1 is biased in saturation. Also assume that the *W/L* ratio of the transistor M2 is *K* time larger than for transistor M1.

a) Derive the output voltage as a function of the *K* factor, i.e., $V_{out} = f(K)$, when the transistor M2 is saturated.Express the output voltages in terms of the current I_0 and transistor design parameters not voltages.

The output voltage is given by $V_{out} = V_{DD} - RI_{D2,\,saturation}$ and the current through transistor M2 when it is saturated is given by (where the channel-length modulation is neglected)

$$I_{D2,\,saturation} = \left(\frac{W_2}{L_2}/\frac{W_1}{L_1}\right)I_{D1} = \left(\frac{W_2}{L_2}/\frac{W_1}{L_1}\right)I_0 = KI_0 \qquad (1.1)$$

Hence,

$$V_{out} = V_{DD} - RKI_0\,. \qquad (1.2)$$

b) Derive the output voltage as a function of the *K* factor, i.e., $V_{out} = g(K)$, when the transistor M2 is operating in the linear region. Express the output voltages in terms of the current I_0 and transistor design parameters not voltages.

The output voltage of the circuit is also here given by

$$V_{out} = V_{DD} - RI_{D2,\,linear}\,, \qquad (1.3)$$

but the current through transistor M2 is given by

$$I_{D2,\,linear} = \beta_2[(V_{GS} - V_{TH})V_{out} - V_{out}^2] = \beta_1 K[(V_{GS} - V_{TH})V_{out} - V_{out}^2]\,. \qquad (1.4)$$

The current through transistor M1 is given by

$$I_D = \frac{\beta_1}{2}(V_{GS} - V_{TH})^2 = \alpha_1(V_{GS} - V_{TH})^2 \quad (1.5)$$

if the channel-length modulation is neglected. Inserting Eq. (1.5) into Eq. (1.4) yields

$$I_{D2,\,linear} = \beta_1 K\left[\sqrt{\frac{I_0}{\alpha_1}}V_{out} - V_{out}^2\right] =$$

$$2K[\sqrt{\alpha_1 I_0}V_{out} - \alpha_1 V_{out}^2] \quad (1.6)$$

Inserting Eq. (1.6) into Eq. (1.3) yields

$$V_{out} = V_{DD} - R2K[\sqrt{\alpha_1 I_0}V_{out} - \alpha_1 V_{out}^2]\,. \quad (1.7)$$

Solving for V_{out} yields

$$V_{out} = \frac{1}{4\alpha_1 KR} + \frac{1}{2}\sqrt{\frac{I_0}{\alpha_1}} \pm \sqrt{\left(\frac{1}{4\alpha_1 KR} + \frac{1}{2}\sqrt{\frac{I_0}{\alpha_1}}\right)^2 - \frac{V_{DD}}{2\alpha_1 KR}} \quad (1.8)$$

c) Determine for which value of K the transistor M2 switches from operating in the saturation region to the linear region.

The K for which the transistor M2 enters the linear operation region from the saturation region is when its drain-source voltage equals the gate-source voltages minus the threshold voltage, i.e.,

$$V_{DS} = V_{GS} - V_T\,. \quad (1.9)$$

In this case it is translated to

$$V_{out} = V_{GS} - V_T = \sqrt{\frac{I_0}{\alpha_1}} \quad (1.10)$$

since the transistors are operating in the saturation region (or both the transistor equations are equal). Further, the output voltage is

$$V_{out} = V_{DD} - RI_{D2,\,saturation} = V_{DD} - RKI_0\,. \quad (1.11)$$

Combining Eq. (1.10) and Eq. (1.11) yields

$$\sqrt{\frac{I_0}{\alpha_1}} = V_{DD} - RKI_0 \quad (1.12)$$

which is reformulated to

$$K = \frac{V_{DD} - \sqrt{\frac{I_0}{\alpha_1}}}{RI_0} = \frac{V_{DD}}{RI_0} - \frac{1}{R\sqrt{\frac{I_0}{\alpha_1}}} \tag{1.13}$$

d) Sketch the output voltage as a function of the K, i.e., $V_{out} = h(K)$, for $K > 0$.

As long as the transistor is operating in the saturation region the output voltage will decrease linearly with increased K value. The output voltage for very small transistor widths will be close to V_{DD}. For very large values of the transistor the output current will be close to ground. When the transistor is operating in the linear operation region the current increase at a lower rate than for the transistor operating in the saturation region. Hence, the slope of the output voltage will decrease as the K value is increased even further.

2. Small-signal analysis

The circuit shown in the figure is used in an analog circuit where each transistor is biased in the saturation region. Further, the size of transistors M2 and M3 are equal. Neglect the influence of all internal parasitics in the transistors.

a) Derive the transfer function of the circuit, i.e., $H(s) = V_{out}(s)/V_{in}(s)$.

The small-signal model of the amplifier is shown in Figure 2.1

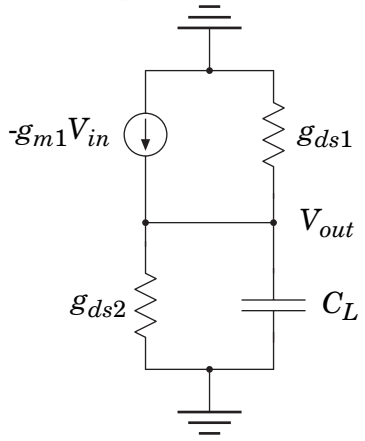

Figure 2.1 The small-signal model of the common-source amplifier biased with a current mirror. (no variations on the current mirror gives AC ground)

Using nodal analysis of the circuit yields

$$V_{out}(g_{ds1} + g_{ds2} + sC_L) + V_{in}g_{m1} = 0. \tag{2.1}$$

Hence, the transfer function is given by

$$H(s) = \frac{V_{out}}{V_{in}} = -\frac{g_{m_1}}{g_{ds1} + g_{ds2} + sC_L} =$$

$$-\frac{g_{m1}}{g_{ds1} + g_{ds2}} \frac{1}{1 + \frac{s}{\frac{g_{ds1} + g_{ds2}}{C_L}}}. \tag{2.2}$$

The DC gain is given by

$$A_0 = -\frac{g_{m1}}{g_{ds1} + g_{ds2}} \propto \frac{\sqrt{\frac{W_1}{L_1} I_{D2}}}{\left(\frac{1}{L_1} + \frac{1}{L_2}\right) I_{D2}} = \frac{1}{2}\sqrt{\frac{W_1 L}{I_{D2}}} \tag{2.3}$$

while the first pole is located at

$$p_1 = \frac{g_{ds1} + g_{ds2}}{C_L} \propto \frac{\left(\frac{1}{L_1} + \frac{1}{L_2}\right) I_{D2}}{C_L} = \frac{1}{2}\frac{I_{D2}}{L C_L} \tag{2.4}$$

and the unity-gain frequency is

$$\omega_u = |A_0| p_1 = \frac{g_{m1}}{C_L} \propto \frac{\sqrt{\frac{W_1}{L} I_{D2}}}{C_L} \tag{2.5}$$

where the channel length of all transistors are assumed to be equal. The output range is given by

$$OR = [V_{ds,\,sat2}; V_{DD} - V_{ds,\,sat1}] = \left[\sqrt{\frac{I_{D2}}{\alpha_2}}; V_{DD} - \sqrt{\frac{I_{D2}}{\alpha_1}}\right] \tag{2.6}$$

Derive expressions for the circuit's output range, common-mode range, DC gain, first pole, and the unity-gain frequency. From these results how will these parameters be affected if...

b) ... *W/L* of the transistors are constant, but *L* (and W) is increased*?*

c) ... the bias current, I_{bias}, is increased?

Table 1: Performance metrics variations due to design parameter variations.

	A0	p1	wu	OR
b) W, L increased	increased	decreased	-	-
c) I_{bias} increased	decreased	increased	increased	decreased

3. Macro blocks

In an analog circuit the building block shown in Figure 3.1 is identified.

a) Derive the transfer function from the input to the output of the circuit, $H(s) = V_{out}(s)/V_{in}(s)$.

The transfer function can be derived into several partial transfer functions (see Figure 3.1).

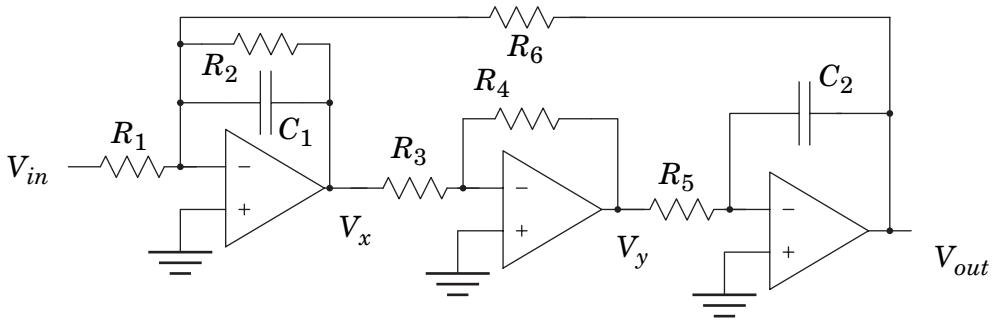

Figure 3.1 A Tow-Thomas biquad.

$$V_{out}(s) = -\frac{1}{sC_2R_5}V_y(s) \tag{3.1}$$

$$V_y(s) = -\frac{R_4}{R_3}V_x(s) \tag{3.2}$$

$$V_x(s) = -\frac{R_2}{R_1(1+sR_2C_1)}V_{in}(s) - \frac{R_2}{R_6(1+sR_2C_1)}V_{out}(s) \tag{3.3}$$

Substituting Eq. (3.2) and Eq. (3.3) into Eq. (3.1) yields

$$V_{out}(s) = -\frac{1}{sC_2R_5}\frac{R_4}{R_3}\left(\frac{R_2}{R_1(1+sR_2C_1)}V_{in}(s) + \frac{R_2}{R_6(1+sR_2C_1)}V_{out}(s)\right)$$

which is reformulated to

$$V_{out}(s)\left(1 + \frac{1}{sC_2R_5}\frac{R_4}{R_3}\frac{R_2}{R_6(1+sR_2C_1)}\right) = -\frac{1}{sC_2R_5}\frac{R_4}{R_3}\frac{R_2}{R_1(1+sR_2C_1)}V_{in}(s)$$

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{-\frac{1}{sC_2R_5}\frac{R_4}{R_3}\frac{R_2}{R_1(1+sR_2C_1)}}{1 + \frac{1}{sC_2R_5}\frac{R_4}{R_3}\frac{R_2}{R_6(1+sR_2C_1)}} = -\frac{R_2}{R_1}\frac{R_4R_6}{(1+sR_2C_1)sC_2R_3R_5R_6 + R_2R_4} =$$

$$-\frac{R_2}{R_1}\frac{R_4R_6}{R_2R_4 + sC_2R_3R_5R_6 + s^2C_1C_2R_2R_3R_5R_6}$$

b) Consider only the second stage, consisting of the resistors R_3 and R_4 and the OP, assume that the OP has a gain of A. Derive the transfer function of this second stage with the non-ideal OP.

The negative input node, V_n, will track the output of the OP, V_y according to Figure 3.1, according to

$$V_y = A(V_p - V_n) \Rightarrow V_n = -\frac{V_y}{A} \tag{3.4}$$

since V_p is connected to analog ground. Using nodal analysis in the negative input node yields

$$\frac{V_x - V_n}{R_3} = \frac{V_n - V_y}{R_4} \tag{3.5}$$

Some manipulations lead to

$$V_y = -\frac{1}{\frac{R_3}{R_4} + \frac{1}{A}\left(1 + \frac{R_3}{R_4}\right)} V_x \tag{3.6}$$

which is simplified to

$$\frac{V_y}{V_x} = -\frac{R_4}{R_3}\frac{1}{1 + \frac{1}{A}\left(1 + \frac{R_4}{R_3}\right)}. \tag{3.7}$$

Hence, increasing R_4 while keeping R_3 constant yields larger errors between the ideal and the non ideal amplifier.

4. Switched-capacitor circuit analysis

A switched capacitor circuit in clock phase 1 is shown in the figure. The value of V_2 changes only at time t, $t + 2\tau$, $t + 4\tau$, and so on, i.e., $V_1(t) = V_1(t + \tau)$.

a) Express the output voltage, $V_{out}(z)$, for clock phase 1 of the switched capacitor circuit shown in Figure 4.1. Assume that the OTA is ideal.

In the first clock cycle we have that

$q_1(t) = C_1(0 - V_x(t))$, $q_2(t) = C_2(0 - V_x(t))$, $q_3(t) = C_3(V_2(t) - V_x(t))$, $q_4(t) = C_4(0 - V_2(t))$

In the clock cycle $t + \tau$

$q_1(t + \tau) = C_1 V_1(t + \tau)$, $q_2(t + \tau) = 0$, $q_3(t + \tau) = q_3(t)$, $q_4(t + \tau) = C_4(0 - V_2(t + \tau))$.

and in clock cycle $t + 2\tau$

$q_1(t + 2\tau) = C_1(0 - V_x(t + 2\tau))$, $q_2(t + 2\tau) = C_2(0 - V_x(t + 2\tau))$, $q_3(t + 2\tau) = C_3(V_2(t + 2\tau) - V_x(t + 2\tau))$, $q_4(t + 2\tau) = C_4(0 - V_2(t + 2\tau))$.

The charge conservation equations are

$$q_2(t) + q_4(t) = q_2(t + \tau) + q_4(t + \tau) \tag{4.1}$$

$$q_2(t + \tau) = q_2(t + 2\tau) \tag{4.2}$$

$$q_1(t + \tau) + q_2(t + \tau) + q_3(t + \tau) = q_1(t + 2\tau) + q_2(t + 2\tau) + q_3(t + 2\tau) \tag{4.3}$$

The Eq. (4.2) yields

$$0 = C_2(0 - V_x(t + 2\tau)) \tag{4.4}$$

which means that $V_x(t + 2\tau) = 0$. Which means that $V_x = 0$ for all times. Furthermore, Eq. (4.1) yields

$$C_2(0 - V_x(t)) + C_4(0 - V_2(t)) = 0 + C_4(0 - V_2(t + \tau)) \tag{4.5}$$

which gives that $V_2(t + \tau) = V_2(t)$. The Eq. (4.3) together with Eq. (4.2) yields

$$\begin{aligned} &C_1V_1(t + \tau) + C_3V_2(t + \tau) = \\ &C_1(0 - V_x(t + 2\tau)) + C_3(V_2(t + 2\tau) - V_x(t + 2\tau)) \end{aligned} \tag{4.6}$$

which is simplified to

$$C_1V_1(t + \tau) + C_3V_2(t) = C_3V_2(t + 2\tau). \tag{4.7}$$

Since $V_1(t + \tau) = V_1(t)$ is given in the exercise this yields that when performing a Z-transformation on Eq. (4.7) the results will be

$$C_1V_1(z) + C_3V_2(z) = zC_3V_2(z) \tag{4.8}$$

rearranging the equation yields

$$\frac{V_2(z)}{V_1(z)} = \frac{C_1}{C_3}\frac{1}{z - 1} \tag{4.9}$$

which is a common non inverting accumulator.

b) Is the circuit insensitive to capacitive parasitics? Motivate your answer carefully.

The parasitics of interest is shown in

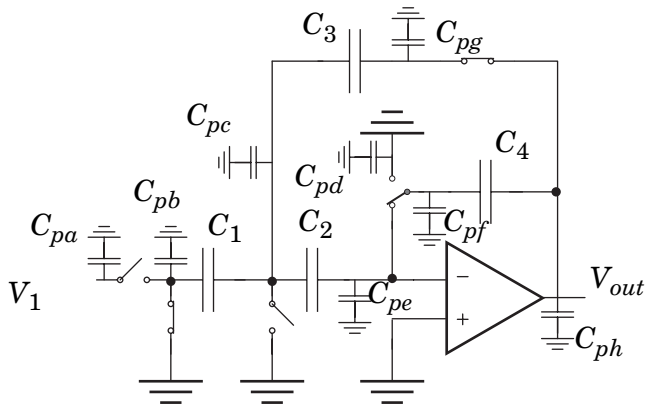

Figure 4.1 The SC circuit with capacitive parasitics due to the capacitor and the switches.

C_{pa} does not alter the transfer function since it is always connected to the ideal input source.

C_{pb} does not change the transfer function since it is shorted to ground in one clock phase and connected to ground and the input source in the other clock phase.

C_{pc} The voltage in node where this parasitics is connected is always virtual

ground. Hence, the transfer function will not be changed.

C_{pd} Connected between ground and ground which results in no change in the transfer function

C_{pe}, C_{pf} Connected between virtual ground and ground. No effect on the transfer function.

C_{pg} Floating node and ground or output node of OP to ground. No changes in the transfer function.

C_{ph} Connected to the output of the OP and ground not changing the transfer function.

Hence, the circuit is insensitive to capacitive parasitics, when the transfer function is of concern, but the settling time will be affected.

5. A mixture of questions

a) Explain the similarities and differences between an operational amplifier and an operational transconductance amplifier.

Both operational amplifiers (OP) and operational transconductance amplifiers (OTY) have high gain, high input impedance and they differ in the output resistance, since an OP has low output resistance while an OTA has high output impedance.

b) What is the difference between a mosfet-C and an active-RC integrator?

An active-RC integrator consists of an operational amplifier and a resistor at the negative input and a capacitor between the output and the negative input. A mosfet-C integrator is the resistor replaced by a mosfet transistor instead.

c) Compare a telescopic-cascode and a folded-cascode OTA with respect to swing, DC gain, and maximum possible unity-gain frequency. Motivate your answers carefully.

In a telescopic-cascode OTA we have 5 transistor on top of each other this means lower swing compared to a folded-cascode OTA which only has 4 transistor stacked on top of each other. The DC gain is approximately the same since these are two single stage OTA which has the gain of g_m/g_{out} where the output resistance is approximately equal (cascoded output stages). The maximum unity-gain frequency is limited by the second pole for a realistic phase margin. The second pole is determined by the amount of capacitive load at the internal nodes. The parasitics load for the folded-cascode amplifier is larger than for the telescopic cascode which means that the telescopic-cascode OTA should have higher maximum unity-gain frequency.

d) Derive the output range of the amplifier shown in the figure.

The maximum possible output voltage so that all transistors are operating in the saturation region is given by

$$V_{out,\,max} = V_{DD} - V_{ds,\,sat,\,7} - V_{ds,\,sat,\,2} =$$
$$= V_{DD} - \sqrt{\frac{I_{D7}}{\alpha_7}} - \sqrt{\frac{I_{D7}}{2\alpha_2}} \qquad (5.1)$$

while the minimum possible output voltage so that all transistors are operating in the saturation region is

$$V_{out,\,min} = max\{V_{gs6} + V_{ds,\,sat,\,4};(V_{ds,\,sat,\,5} + V_{gs3} - V_{gs4} + V_{ds,\,sat,\,4})\} =$$

$$= max\left\{\sqrt{\frac{I_{D7}}{2\alpha_6}} + V_{T6} + \sqrt{\frac{I_{D7}}{2\alpha_4}};\left(\sqrt{\frac{I_{D7}}{2\alpha_5}} + \sqrt{\frac{I_{D7}}{2\alpha_3}} + V_{T3} - V_{T4}\right)\right\}$$

e) State three benefits of using active load instead of passive load in a CMOS amplifier?

Smaller silicon area, larger possible swing, and high output impedance => high DC gain.

f) A three terminal switch, the figure (a), is realized with two NMOS devices, the figure (b), in an SC circuit. The gates of the transistors are connected to the clocks, ϕ_1 and ϕ_2, respectively. The waveforms for two different types of 2-phase clocks are shown in the figure (c) and (d), where ϕ_1 is solid and ϕ_2 is dashed. Which of these two 2-phase clocks((c) or (d)) should be used in order to guarantee a good operation of the SC circuit. Motivate your answer carefully.

(d) is the correct operation since otherwise both of the switches will be on at the same time which is not the desired operation. Hence, we like to have non overlapping clocks in order to guarantee good operation.