Written Test
TSEI30,
Analog and Discrete-time Integrated Circuits

Date	August 26, 2002
Time:	14 - 18
Max. no of points:	70; 50 from written test, 15 for project, and 5 the assignment.
Grades:	30 for 3, 42 for 4, and 56 for 5.
Allowed material:	All types of calculators except Lap Tops. All types of tables and handbooks. The textbook Johns & Martin: Analog Integrated Circuit Design
Examiner:	Lars Wanhammar.
Responsible teacher:	Robert Hägglund. Tel.: 013 - 28 16 76 (3).
Correct (?) solutions:	Solutions and results will be displayed in House B, entrance 25 - 27, 1st floor.

Good Luck!

Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

Solutions

1. Basic building block

a) Starting from V_{DD} we know that the transistor is cut-off when the $V_{SG} < V_T$. Hence, no current (only the very small leakage current) will flow through the transistor and thereby the output voltage will be very close to ground.

Decreasing the input voltage will set the transistor to operating in the saturation region. The current will approximately increase quadratically and thereby will the output voltage increase quadratically. At a certain voltage when $V_{SG} < V_{SG} - V_T > 0$ then will the transistor start to operate in the linear region and the current will increase linearly. The output voltage will increase linearly until it is close to V_{DD}.

b) The current in the saturation region of the transistor is given by

$$I_D = \alpha(V_{SG} - V_T)^2(1 + \lambda V_{DS})$$

Assuming that the channel length modulation is negligible yields the following equation

$$I_D = \alpha(V_{DD} - V_{in} - V_T)^2 \tag{1.1}$$

The current through the resistor is given by

$$I_R = \frac{V_{out}}{R} \tag{1.2}$$

We know that the maximum voltage for the transistor to operate in the saturation region is $V_{DD} - V_T$. For the transition from the saturation to linear (triode) region we know that $V_{SD} = V_{SG} - V_T$ which is equal to $V_{DD} - V_{out} = V_{DD} - V_{in} - V_T$. Adding these expressions gives

$$\frac{V_{out}}{R} = \alpha(V_{DD} - V_{out})^2 \tag{1.3}$$

solving the equation yields the result of the maximum output voltage for the

transistor to be in saturation.

$$V_{out} = V_{DD} + \frac{1}{2R\alpha} \pm \sqrt{\frac{V_{DD}}{R\alpha} + \frac{1}{4R^2\alpha^2}} \tag{1.4}$$

We know that the solution with $V_{out} > V_{DD}$ is a false solution. The minimum input voltage so that the transistor is operating in the saturation region is $V_{in} = V_{out} - V_{TH}$. Hence,

$$V_{DD} + \frac{1}{2R\alpha} - \sqrt{\frac{V_{DD}}{R\alpha} + \frac{1}{4R^2\alpha^2}} - V_T < V_{in} < V_{DD} - V_T \tag{1.5}$$

2. Small signal analysis

a) The small signal model of the double cascode amplifier is shown in Figure 2.1

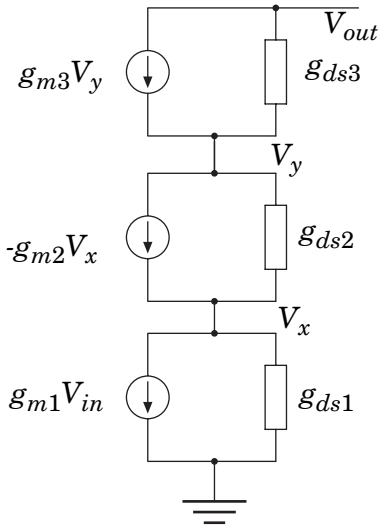

Figure 2.1 The small signal model of the amplifier.

Using nodal analysis in nodes V_{out}, V_y, and V_x yields the following equations

$$g_{m3}V_y + (V_y - V_{out})g_{ds3} = 0 \tag{2.1}$$

$$g_{m3}V_y + (V_y - V_{out})g_{ds3} + (V_y - V_x)g_{ds2} - g_{m2}V_x = 0 \tag{2.2}$$

$$(V_y - V_x)g_{ds2} - g_{m2}V_x - V_x g_{ds1} - g_{m1}V_{in} = 0 \tag{2.3}$$

Solving for V_y in Eq. (2.1) yields

$$V_y = \frac{g_{ds3}}{g_{m3} + g_{ds3}} V_{out} \tag{2.4}$$

inserting this in Eq. (2.2) and then solving for V_x gives

$$\left((g_{m3}+g_{ds3}+g_{ds2})\frac{g_{ds3}}{g_{m3}+g_{ds3}}-g_{ds3}\right)V_{out} = V_x(g_{m2}+g_{ds2})$$

which can be simplified and rearranged to

$$V_x = \frac{g_{ds2}g_{ds3}}{(g_{m3}+g_{ds3})(g_{m2}+g_{ds2})}V_{out} \tag{2.5}$$

and finally inserting these equations into Eq. (2.3) and solving for V_{out} gives the transfer function.

$$\left(\frac{g_{ds2}g_{ds3}}{g_{m3}+g_{ds3}}-(g_{m2}+g_{ds2}+g_{ds1})\frac{g_{ds2}g_{ds3}}{(g_{m3}+g_{ds3})(g_{m2}+g_{ds2})}\right)V_{out} = g_{m1}V_{in}$$

Simplify the expression gives

$$-\frac{g_{ds1}g_{ds2}g_{ds3}}{(g_{m3}+g_{ds3})(g_{m2}+g_{ds2})}V_{out} = g_{m1}V_{in} \tag{2.6}$$

The transfer function is given by

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m1}}{\frac{g_{ds1}g_{ds2}g_{ds3}}{(g_{m3}+g_{ds3})(g_{m2}+g_{ds2})}} = \frac{-g_{m1}}{g_{out}} \tag{2.7}$$

By approximating this expression we get

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m1}g_{m2}g_{m3}}{g_{ds1}g_{ds2}g_{ds3}} \tag{2.8}$$

b) How to increase the DC gain by changing certain design parameters can be found by expressing g_m and g_{ds} in the large signal parameters.

$$g_m \propto \sqrt{\frac{W}{L}I_{bias}} \tag{2.9}$$

and

$$g_{ds} \propto \frac{I_{bias}}{L} \tag{2.10}$$

Inserting these equation into Eq. (2.8) gives the following expression for the DC gain

$$A_0 = \left.\frac{V_{out}}{V_{in}}\right|_{s=0} = \frac{\sqrt{\frac{W_1}{L}I_{bias}}\sqrt{\frac{W_2}{L}I_{bias}}\sqrt{\frac{W_3}{L}I_{bias}}}{\frac{I_{bias}}{L}\frac{I_{bias}}{L}\frac{I_{bias}}{L}} =$$

$$= \frac{\sqrt{W_1W_2W_3}(I_{bias}L)^{3/2}}{I_{bias}^3} = \sqrt{W_1W_2W_3}\left(\frac{L}{I_{bias}}\right)^{3/2} \qquad (2.11)$$

The DC gain can be increased by a factor of two by decreasing the bias current. I_{bias} must be decreased by a factor of $2^{2/3}$ to obtain a doubled DC gain.

c) The double cascoded configuration we have a lower power consumption compared to a gain boosted version for equal DC gain, but the output swing will be lower for the double cascode.

3. An amplifier in a context

a) The transfer function is found by using KCL at the negative input terminal of the amplifier.

$$(V_{in} - V_n)G_1 + (V_{out} - V_n)sC_1 = 0 \qquad (3.1)$$

Furthermore, the output voltage of the amplifier is expressed as

$$V_{out} = (V_p - V_n)A(s) = A(s)(0 - V_n) = -\frac{A_0}{1 + \frac{s}{p_1}}V_n \qquad (3.2)$$

Combining Eq. (3.1) and Eq. (3.2) and eliminating V_n yields the following transfer function.

$$\frac{V_{out}}{V_{in}} = -\frac{G_1}{sC_1 + (sC_1 + G_1)\frac{1 + \frac{s}{p_1}}{A_0}} = -\frac{A_0}{1 + s\left(\frac{C_1(1 + A_0)}{G_1} + \frac{1}{p_1}\right) + s^2\frac{C_1}{p_1G_1}}$$

In the design we know that $C_1R_1 > 1/p_1$ which yields that $C_1(1 + A_0)R_1 \gg 1/p_1$ since an operational amplifier has large gain.
This leads to that the poles of the closed loop system can be extracted from the expression above.

$$p_I \approx \frac{G_1}{C_1(1 + A_0)} \approx \frac{G_1}{A_0C_1} \qquad (3.3)$$

and

$$p_{II} \approx \frac{A_0C_1}{G_1}\frac{p_1G_1}{C_1} = A_0p_1 \approx \omega_{u,\,amplifier} \qquad (3.4)$$

by using the approximation that

$$\left(1+\frac{s}{p_I}\right)\left(1+\frac{s}{p_{II}}\right) = 1 + s\left(\frac{1}{p_I}+\frac{1}{p_{II}}\right) + \frac{s^2}{p_I p_{II}} \approx 1 + \frac{s}{p_I} + \frac{s^2}{p_I p_{II}}$$

and identify with the expression for the transfer function. The DC gain of the circuit is equal to the DC gain of the open loop amplifier.

b) The phase margin is defined as the phase plus 180 degrees at the unity-gain frequency. The phase is

$$\phi = -\text{atan}\frac{\omega}{p_I} - \text{atan}\frac{\omega}{p_{II}} \tag{3.5}$$

The unity-gain frequency is approximately given by

$$\omega_{u,\,integrator} \approx A_{0,\,integrator} p_I = A_0 \frac{G_1}{A_0 C_1} = \frac{G_1}{C_1} = \frac{1}{R_1 C_1} \tag{3.6}$$

Hence, the phase margin is given by

$$\phi_m = \phi + 180 = -\text{atan}\frac{p_I A_0}{p_I} - \text{atan}\frac{A_0 p_I}{p_{II}} + 180 =$$

$$180 - \text{atan}\,A_0 - \text{atan}\frac{p_I}{p_1} \tag{3.7}$$

where p_1 is the first pole of the amplifier and P_I is the first pole of the integrator.

In an ideal integrator we have a phase margin of 90 degrees. In Eq. (3.7) we see that the second term is approximately equal to 90 degrees and thereby we need to ensure that p_I/p_1 must be a small value. Hence, we have to have a large value of the first pole of the amplifier compared to the first pole of the integrator to have a good integrator.

4. Switched capacitor circuit

A switched capacitor circuit in clock cycle 1 is shown in the figure.

a) Derive the transfer function for the clock cycle 1 of the switched capacitor circuit, i.e., $V_{out}(z)/V_{in}(z)$. Assume that the OTA is ideal.

The circuit in Figure 4.1 shows the circuit for both clock cycles.

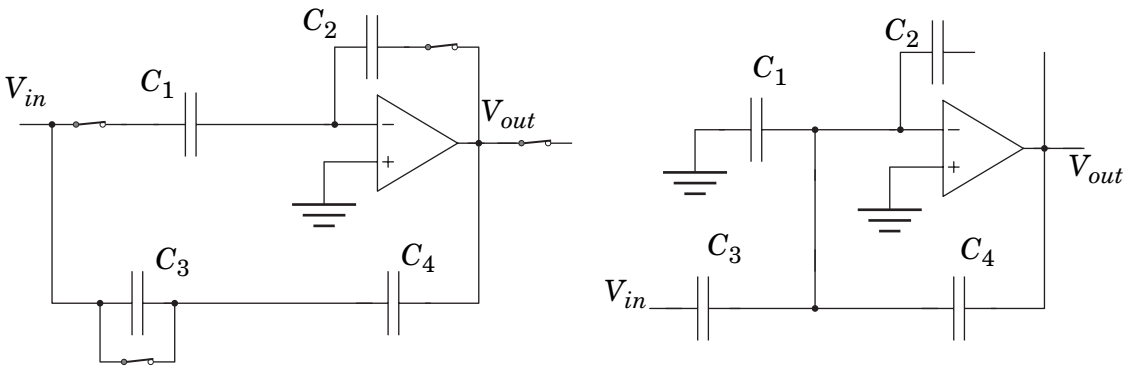

Figure 4.1 The SC circuit in both clock phases. Left ϕ_1, Right ϕ_2.

To compute the transfer function for the circuit charge redistribution analysis is used.

For clock cycle 1, ϕ_1, at time t

$q_1(t) = C_1(V_{in}(t) - 0)$; $q_2(t) = C_2(V_{out}(t) - 0)$; $q_3(t) = 0$;
$q_4(t) = C_4(V_{out}(t) - V_{in}(t))$

For clock cycle 2, ϕ_2, at time $t + \tau$

$q_1(t + \tau) = 0$; $q_2(t + \tau) = q_2(t)$;
$q_3(t + \tau) = C_3(V_{in}(t + \tau) - 0)$ $q_4(t + \tau) = C_4(V_{out}(t + \tau) - 0)$

The charge on the plates of capacitor C_2 will be unchanged since it is not connected on both terminals during clock phase 2.

For clock cycle 1, ϕ_1, at time $t + 2\tau = t + T$:

$q_1(t + 2\tau) = C_1(V_{in}(t + 2\tau) - 0)$; $q_2(t + 2\tau) = C_2(V_{out}(t + 2\tau) - 0)$;
$q_3(t + 2\tau) = 0$ $q_4(t + 2\tau) = C_4(V_{out}(t + 2\tau) - V_{in}(t + 2\tau))$

The charge conservation equations are

$$q_1(t) + q_2(t) + q_3(t) + q_4(t) = q_1(t + \tau) + q_2(t + \tau) + q_3(t + \tau) + q_4(t + \tau)$$

$$q_1(t + \tau) + q_2(t + \tau) = q_1(t + 2\tau) + q_2(t + 2\tau)$$

Inserting the charges into the lower one of the equations above gives the following expression

$$0 + C_2 V_{out}(t) = C_1 V_{in}(t + 2\tau) + C_2 V_{out}(t + 2\tau)$$

Perform Z transformation on the expression gives

$$-C_1 z V_{in}(z) = C_2(z - 1) V_{out}(z)$$

The transfer function is then

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = -\frac{C_1}{C_2}\frac{z}{z - 1} = -\frac{C_1}{C_2}\frac{1}{1 - z^{-1}} \qquad (4.1)$$

It is a inverting accumulator

b) Is the circuit insensitive to capacitive parasitics? Motivate your answer carefully.

The circuit with parasitic capacitors are shown in

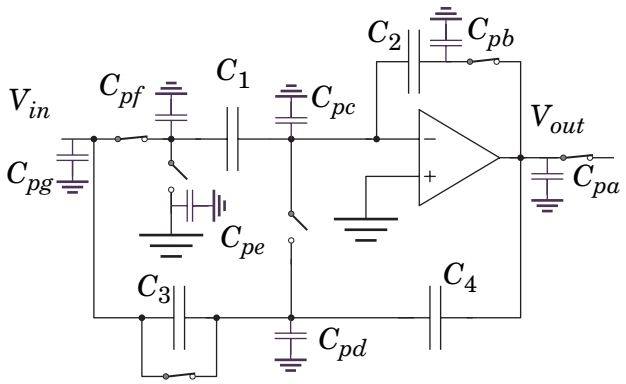

Figure 4.2 The SC circuit with parasitics capacitors

C_{pa} is connected to the ideal output of the OPamp and ground and thereby not changing the transfer function.

C_{pb} Charged by the output of the operational amplifier in clock cycle 1 and does not discharge during clock cycle 2. Not changing the transfer function.

C_{pc} is connected between the virtual ground and ground and thereby not changing the transfer function.

C_{pd} is charged by the input voltage during clock cycle 1 and discharged during clock cycle 2 into the virtual ground and thereby changing the transfer function.

C_{pe} is connected with both terminal to ground and not changing the transfer function

C_{pf} Connected between ground and the input voltage or ground and ground so it will be charged in clock cycle 1 and discharged to ground in clock cycle 2. Hence, not affecting the transfer function.

C_{pg} Charged by the input source and discharged to ground and thereby not changing the transfer function.

The circuit is sensitive to parasitics since the value of the parasitic capacitor C_{pd} will be a part of the over all transfer function if they are included in the computation of the transfer function.

c)

An offset voltage is modelled as a voltage source at the positive input of the amplifier. The voltage source will have the value of V_{os}.

Performing the charge redistribution analysis gives:

For clock cycle 1, ϕ_1, at time t

$q_1(t) = C_1(V_{in}(t) - V_{os})$; $q_2(t) = C_2(V_{out}(t) - V_{os})$; $q_3(t) = 0$;
$q_4(t) = C_4(V_{out}(t) - V_{in}(t))$

For clock cycle 2, ϕ_2, at time $t + \tau$

$q_1(t + \tau) = -C_1 V_{os}$; $q_2(t + \tau) = q_2(t)$;
$q_3(t + \tau) = C_3(V_{in}(t + \tau) - V_{os})$ $q_4(t + \tau) = C_4(V_{out}(t + \tau) - V_{os})$

The charge on the plates of capacitor C_2 will be unchanged since it is not connected on both terminals during clock phase 2.

For clock cycle 1, ϕ_1, at time $t + 2\tau = t + T$:

$q_1(t + 2\tau) = C_1(V_{in}(t + 2\tau) - V_{os})$; $q_2(t + 2\tau) = C_2(V_{out}(t + 2\tau) - V_{os})$;
$q_3(t + 2\tau) = 0$ $q_4(t + 2\tau) = C_4(V_{out}(t + 2\tau) - V_{in}(t + 2\tau))$

The charge conservation equations are

$$q_1(t) + q_2(t) + q_3(t) + q_4(t) = q_1(t+\tau) + q_2(t+\tau) + q_3(t+\tau) + q_4(t+\tau)$$

$$q_1(t+\tau) + q_2(t+\tau) = q_1(t+2\tau) + q_2(t+2\tau)$$

Inserting the charges into the lower one of the equations above gives the following expression

$-C_1V_{os} + C_2(V_{out}(t) - V_{os}) =$
$C_1(V_{in}(t+2\tau) - V_{os}) + C_2(V_{out}(t+2\tau) - V_{os})$

Here we can see that the V_{os} can be cancelled. Hence, the transfer function is the same in exercise a.

5. A mixture of questions

a)

Accurate matching is achieved if we are using unit sized elements or elements with at least the same area or perimeter ration. Furthermore, the area to perimeter for the unit sized capacitors should be as large as possible.

Using common-centroid layout techniques makes the capacitor array less sensitive to temperature gradient and slow oxide thickness variations.

Another important point is to ensure that the neighborhood of each capacitor is equal. This is done by adding dummy capacitor around the capacitor array.

Matching of components depends of the distance of the devices. Hence, a structure with as short maximum distance is desired.

b)

The process technology can make it impossible to have two different voltages at the bulk of two transistors, as our case (M1, M2 and M5).

It is not possible to connect the bulk of transistor M1 and M2 to the substrate if we are not using an p-well in a p-substrate process. It comes from the fact that there is low resistance between the substrate contacts of the three transistors.

It is possible to implement this amplifier in n-substrate and the twin well process but not the n-substrate and P-well process.

c)

The positive PSRR is found by adding an ac source at the positive power supply line and compute the transfer function to the output. By taking the absolute value and dividing the transfer function from the input to the output with the transfer function from the positive power supply to the output we achieve the positive PSRR.

The transfer function from the input to the output is given by

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m1}}{g_{ds1} + g_{ds2}} \qquad (5.1)$$

The transfer function from the positive power supply to the output is given by

$$\frac{V_{out}}{V_{ps}} = \frac{g_{m2} + g_{ds2}}{g_{ds1} + g_{ds2}} \tag{5.2}$$

Hence, the positive PSRR equals

$$pPSRR = \frac{g_{m1}}{g_{m2} + g_{ds2}} \tag{5.3}$$

d) Transistors in the saturation region have higher transconductance and about the same output conductance. Hence, the gain of the circuit will be much higher if both transistor are operating in the saturation region.

e) A CMFB, Common-Mode Feed Back, circuit is used to stabilize the output voltage of a fully differential circuit.