Written Test
TSEI30,
Analog and Discrete-time Integrated Circuits

Date:	Mars 10, 2004
Time:	14 – 18
Place:	KÅR
Max. no of points:	70; 50 from written test, 5 for project, and 15 for assignments.
Grades:	30 for 3, 42 for 4, and 56 for 5.
Allowed material:	All types of calculators except Lap Tops. All types of tables and handbooks. The textbook Johns & Martin: Analog Integrated Circuit Design. Dictionaries.
Examiner:	Lars Wanhammar.
Responsible teacher:	Robert Hägglund. Tel.: 0705 - 48 56 88.
Correct (?) solutions:	Solutions and results will be displayed in House B, entrance 25 - 27, ground floor.

Good Luck!

Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

Exercise

1. Large-signal analysis

The circuit in Figure 1.1 is to be used in an analog circuits. Neglect the influence of the body effect and the channel-length modulation.

a) Derive the voltage V_x as a function of the output voltage, but not as a function of the input voltage. Hint: $I_{R1} = I_{R2}$. (1p)

b) Derive the output voltage as a function of the input voltage when the transistor is saturated. (4p)

c) Derive an equation for the output voltage as a function of the input voltage when the transistor is operating in the linear region. You do not have to solve the equation. (2p)

d) Derive an equation that expresses the output voltage, V_{out}, when the transistor switches from operating in the saturation region to the linear region, as a function the resistances, transistor parameters, and the power supply voltage. You do not have to solve the equation. The equation should be expressed as a polynomial. (3p)

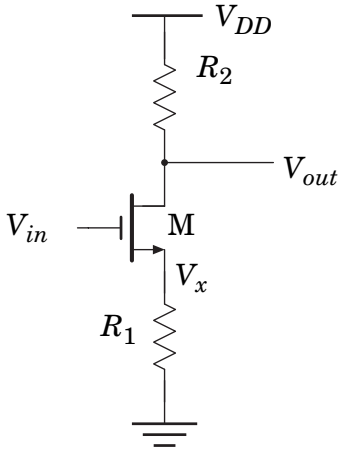

Figure 1.1 A commonly used analog circuit.

2. Small-signal analysis

The transistor in the circuit shown in Figure 2.1 is biased in the saturation region. Neglect the influence of all internal parasitics in the transistor.

a) Draw the small-signal model for the circuit. Do not neglect the bulk effect. (2p)

b) Derive the transfer function of the circuit, i.e., $H(s) = V_{out}(s)/V_{in}(s)$. (3p)

c) Derive approximate expressions for the DC gain, first pole, second pole, zeros, and the output resistance as a function of, e.g., the small-signal parameters, resistances, and capacitances. Assume that $C_L \gg C_{R1}$ and $G_1 \approx G_2 \gg g_m$.

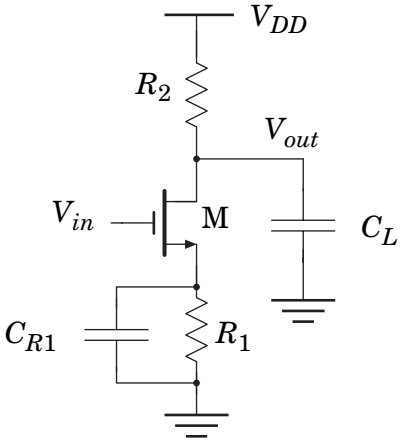

Figure 2.1 Analog CMOS circuit.

3. Macro blocks

In an analog circuit, the building block shown in Figure 3.1 is found. The OP amp is assumed to be ideal except that it has finite DC gain, A_0, and a nonzero output resistance, R_{out}.

a) Derive the transfer function from the input to the output of the circuit, $H(s) = V_{out}(s)/V_{in}(s)$. (4p)

b) Derive the transfer function, $H(s) = V_{out}(s)/V_{in}(s)$, for the circuit when the DC gain is infinite and the output resistance is nonzero. (3p)

c) Derive the transfer function, $H(s) = V_{out}(s)/V_{in}(s)$, of the circuit when the output resistance is zero and the DC gain is finite.

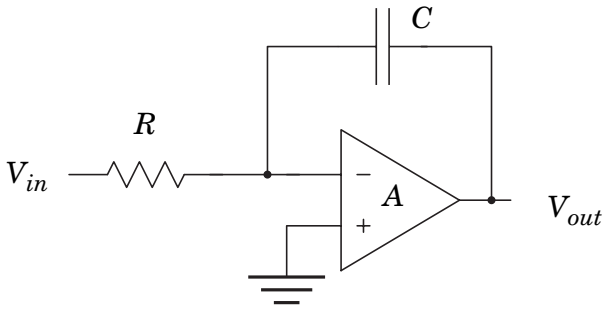

Figure 3.1 An active-RC circuit.

4. Switched-capacitor circuit analysis

A switched capacitor circuit in clock phase 1, i.e., time t, $t + 2\tau$, $t + 4\tau$, is shown in Figure 4.1. The value of V_{in} changes only at time t, $t + 2\tau$, $t + 4\tau$, and so on, i.e., $V_{in}(t) = V_{in}(t + \tau)$.

a) Express the output voltage, $V_{out}(z)$, for clock phase 1 of the switched capacitor circuit shown in Figure 4.1. Assume that the OTA is ideal. (4p)

b) Is the circuit insensitive to capacitive parasitics? Motivate your answer carefully. (2p)

c) Express the output voltage, $V_{out}(z)$, for clock phase 1 of the switched capacitor circuit shown in Figure 4.1. Assume that the OTA suffers from an offset voltage. (4p)

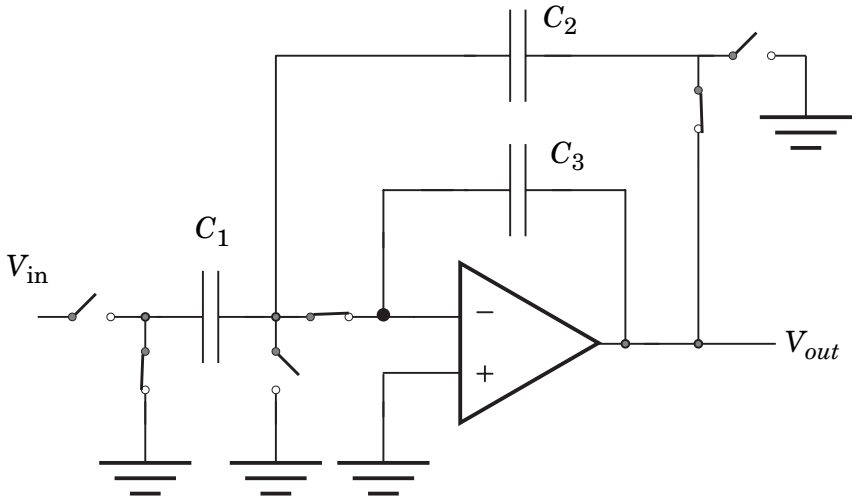

Figure 4.1 A switched-capacitor circuit in clock phase 1.

5. A mixture of questions

a) The current in a special CMOS transistor is given by

$$I = \alpha(V_{GS} - V_T)^{\gamma}(1 + \lambda(V_{DS} - V_{GS} + V_T)) \qquad (5.1)$$

Derive approximate expressions for the transconductance and the output conductance as a function of the current through the device, but not as a function of any voltages. For the computation of the transconductance assume that the λ parameter is zero. (4p)

b) State three techniques to increase the DC gain in the common-source amplifier shown inFigure 5.1. Both changes to the topology and the

design parameters are allowed. (2p)

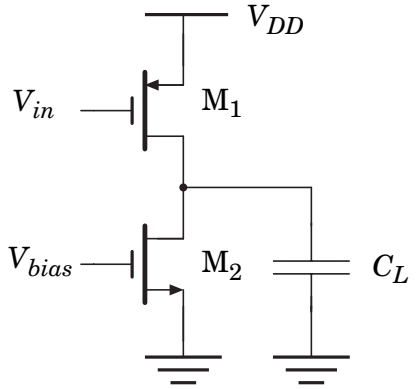

Figure 5.1 A common-source amplifier stage.

c) Derive the input and output ranges of the amplifier shown in Figure 5.2 where all transistors are operating in the saturation region. Express the input and output ranges in relevant design parameters (I_{bias}, α_i, ...). Assume that the size of transistor M8 equals M5, M7 equals M6, M1 equals M2, and M3 equals M4. (4p)

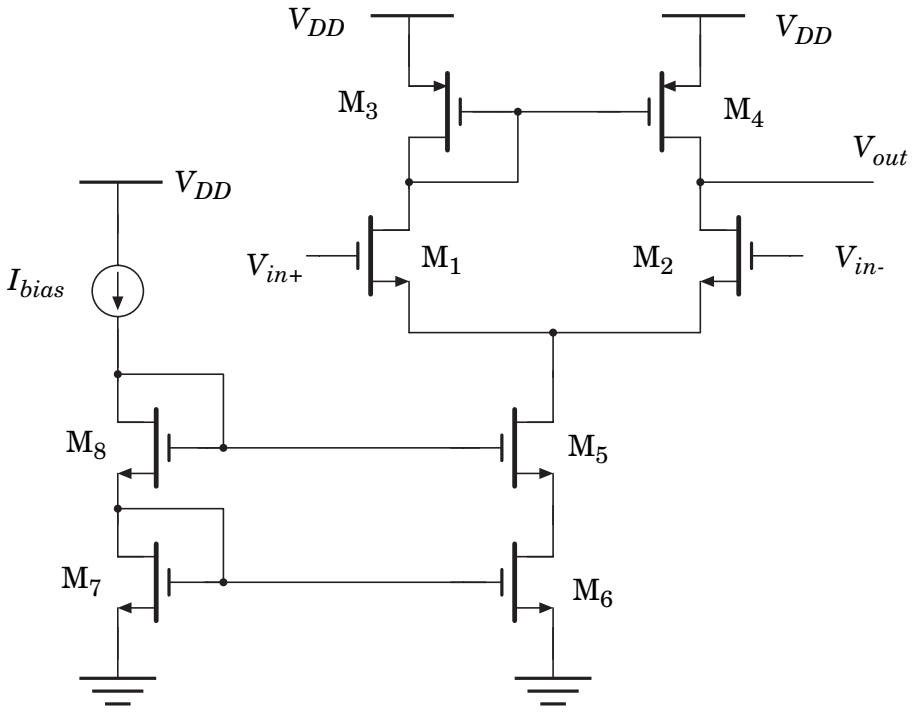

Figure 5.2 A CMOS amplifier circuit.

Transistor formulas and noise

CMOS transistors

Current formulas and operating regions

Cut-off:

$$V_{GS} < V_T \qquad I_D \approx 0$$

Linear:

$$V_{GS} - V_T > V_{DS} > 0 \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (2(V_{GS} - V_T) - V_{DS}) \cdot V_{DS}$$

Saturation:

$$0 < V_{GS} - V_T < V_{DS} \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda V_{DS})$$

Small-signal parameters

Linear region:

$$g_m \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot V_{DS} \qquad g_{ds} \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_T - V_{DS})$$

Saturation region:

$$g_m = \frac{dI_D}{dV_{GS}} \approx \sqrt{2\mu_0 C_{ox} \frac{W}{L} I_D} \qquad g_{ds} = \frac{dI_D}{dV_{DS}} \approx \lambda I_D$$

Circuit noise

Thermal noise

The thermal noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{8kT}{3} \cdot \frac{1}{g_m}$$

Flicker noise

The flicker noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{K}{WLC_{ox}f}$$