Written Test
TSEI30,
Analog and Discrete-time Integrated Circuits

Date	April 29, 2003
Time:	14 – 18
Place:	U14
Max. no of points:	70; 50 from written test, 5 for project, and 15 for assignments.
Grades:	30 for 3, 42 for 4, and 56 for 5.
Allowed material:	All types of calculators except Lap Tops. All types of tables and handbooks. The textbook Johns & Martin: Analog Integrated Circuit Design
Examiner:	Lars Wanhammar.
Responsible teacher:	Robert Hägglund. Tel.: 0705 - 48 56 88.
Correct (?) solutions:	Solutions and results will be displayed in House B, entrance 25 - 27, ground floor.

Good Luck!

Student's Instructions

The CMOS transistor operation regions, small signal parameters, and noise characteristics are found on the last page of this test.

Generally, do not just answer yes or no to a short question. You always have to answer with figures, formulas, etc., otherwise no or fewer points will be given.

Basically, there are few numerical answers to be given in this test.

You may write down your answers in Swedish or English.

Exercise

1. Large-signal analysis

The circuit in Figure 1.1 is a commonly used structure when designing analog circuits. In all following exercises assume that transistor M1 is biased in saturation. Also assume that the *W/L* ratio of transistor M2 is *K* times larger than that of transistor M1.

a) Derive the output voltage as a function of the factor *K*, i.e., $V_{out} = f(K)$, when transistor M2 is saturated. Express the output voltages in terms of the current I_0 and transistor design parameters, but not voltages. (2p)

b) Derive the output voltage as a function of the factor *K*, i.e., $V_{out} = g(K)$, when transistor M2 is operating in the linear region. Express the output voltages in terms of the current I_0 and transistor design parameters, but not voltages (4p)

c) Determine for which value of *K* transistor M2 switches from operating in the saturation region to the linear region. (2p)

d) Sketch the output voltage as a function of the *K*, i.e., $V_{out} = h(K)$, for $K > 0$. (2p)

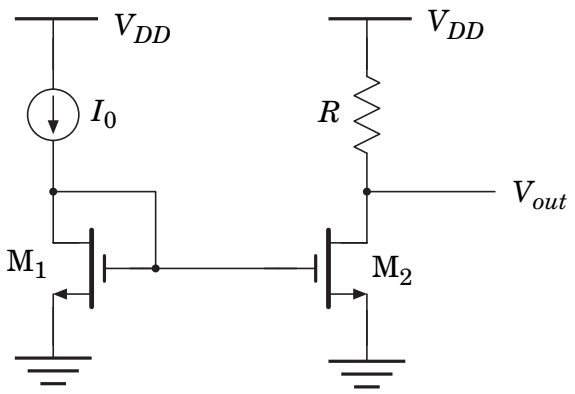

Figure 1.1 A commonly used analog circuit.

2. Small-signal analysis

The circuit shown in Figure 2.1 is used in an analog circuit where each transistor is biased in the saturation region. Further, the size of transistors M2 and M3 are equal and all channel lengths are equal. Neglect the influence of all internal parasitics in the transistors.

a) Derive the transfer function of the circuit, i.e., $H(s) = V_{out}(s)/V_{in}(s)$. (2p)

Derive expressions for the circuit's output range, DC gain, first pole, and the unity-gain frequency. From these results how will these parameters be affected if...

b) ... *W/L* of the transistors are constant, but *L* (and W) is increased*?* (4p)

c) ... the bias current, I_{bias}, is increased? (4p)

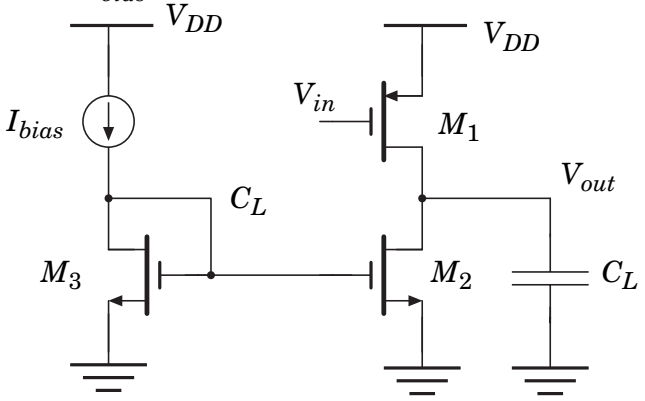

Figure 2.1 Analog CMOS circuit.

3. Macro blocks

In an analog circuit the building block shown in Figure 3.1 is found.

a) Derive the transfer function from the input to the output of the circuit, $H(s) = V_{out}(s)/V_{in}(s)$. (6p)

b) Consider only the second stage, consisting of the resistors R_3 and R_4 and the OP in the middle. Assume that the OP has a gain of *A*. Derive the transfer function of this second stage with the non-ideal OP. The input is the left node of R_3, and the output is the output of the OP. (4p)

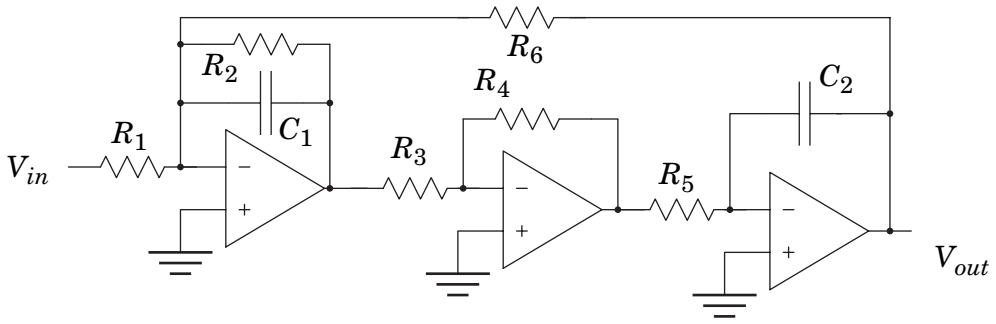

Figure 3.1 An active-RC circuit.

4. Switched-capacitor circuit analysis

A switched capacitor circuit in clock phase 1 is shown in Figure 4.1. The value of V_1 changes only at time t, $t + 2\tau$, $t + 4\tau$, and so on, i.e., $V_1(t) = V_1(t + \tau)$.

a) Express the output voltage, $V_{out}(z)$, for clock phase 1 of the switched capacitor circuit shown in Figure 4.1. Assume that the OTA is ideal. (8p)

b) Is the circuit insensitive to capacitive parasitics? Motivate your answer carefully. (2p)

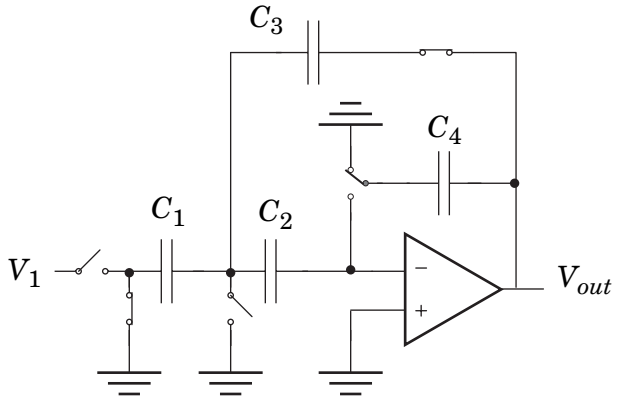

Figure 4.1 A switched-capacitor circuit in clock phase 1.

5. A mixture of questions

a) Explain the similarities and differences between an operational amplifier and an operational transconductance amplifier. (1p)

b) What is the difference between a mosfet-C and an active-RC integrator? (1p)

c) Compare a telescopic-cascode and a folded-cascode OTA with respect to swing, DC gain, and maximum possible unity-gain frequency. Motivate your answers carefully. (3p)

d) Derive the output range of the amplifier shown in Figure 5.1. Express the output range in relevant design parameters (I_{D7}, α_i, ...). (2p)

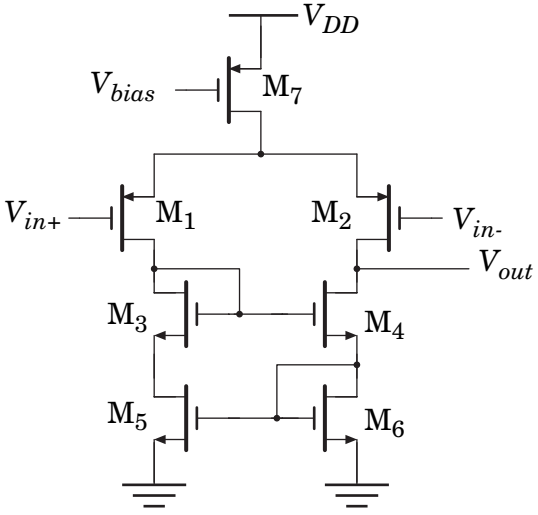

Figure 5.1 A CMOS amplifier circuit.

e) State three benefits of using active load instead of passive load in a CMOS amplifier? (2p)

f) A three terminal switch, Figure 5.2(a), is realized with two NMOS devices, Figure 5.2(b), in an SC circuit. The gates of the transistors are connected to the clocks ϕ_1 and ϕ_2, respectively. The waveforms for two different types of 2-phase clocks are shown in Figure 5.2(c) and (d), where ϕ_1 is solid and ϕ_2 is dashed. Which of these two 2-phase clocks ((c) or (d)) should be used in order to guarantee a good operation of the SC circuit. Motivate your answer carefully. (1p)

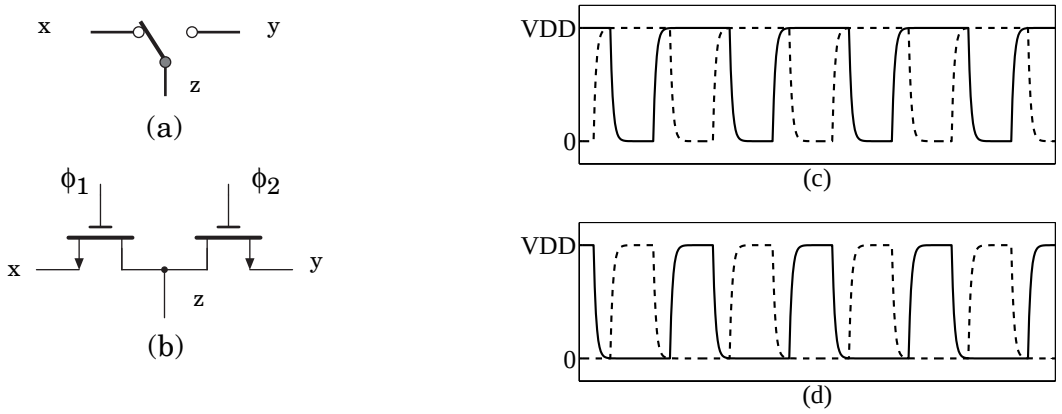

Figure 5.2 (a) A schematic view of a switch within an SC circuit. (b) Transistor implementation of the switch. (c) and (d) two different 2-phase clocks.

Transistor formulas and noise

CMOS transistors

Current formulas and operating regions

Cut-off:

$$V_{GS} < V_T \qquad I_D \approx 0$$

Linear:

$$V_{GS} - V_T > V_{DS} > 0 \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (2(V_{GS} - V_T) - V_{DS}) \cdot V_{DS}$$

Saturation:

$$0 < V_{GS} - V_T < V_{DS} \qquad I_D \approx \frac{\mu_0 C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda V_{DS})$$

Small-signal parameters

Linear region:

$$g_m \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot V_{DS} \qquad g_{ds} \approx \mu_0 C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_T - V_{DS})$$

Saturation region:

$$g_m = \frac{dI_D}{dV_{GS}} \approx \sqrt{2\mu_0 C_{ox} \frac{W}{L} I_D} \qquad g_{ds} = \frac{dI_D}{dV_{DS}} \approx \lambda I_D$$

Circuit noise

Thermal noise

The thermal noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{8kT}{3} \cdot \frac{1}{g_m}$$

Flicker noise

The flicker noise spectral density at the gate of a CMOS transistor is

$$\frac{\overline{v^2}}{\Delta f} = \frac{K}{WLC_{ox}f}$$