TSEI09, Analog Integrated Circuits, 2011-08-24
Written exam, TEN1

Date and time	2011-08-24, 8.00 - 12.00
Location(s)	TER2
Responsible teacher	J Jacob Wikner, jacwi50, +46-70-5915938
Aid	Any written and printed material, including books and old exams. Note! No pocket calculators, no laptops, no iPods, no telephones, no internet connection.
Instructions	A maximum of 25 points can be obtained from the written exam. Three points can be obtained from quizzes. In total: 10 points are required to pass, 15 for a grade four, and 20 for a grade five. ✗ *Hint!* ***Be strategic*** *when you pick exercises to solve. You have five exercises in four hours and you could therefore spend some 45 minutes on each exercise. That leaves you 15 minutes to relax...* Note that a **good motivation to your answer** must be included in your solutions in order to obtain maximum number of points! With "motivation" mathematical derivations are understood (and not only text). Also note that the questions in this exam are divided into logical sections. You may use **Swedish, English or German** in your answers. Notice that some questions are **"hidden" in the text** and therefore: read the instructions carefully! ✗ *Notice also that eventhough you do not fully know the answer, please add some elaborations on your reasoning around the question. Any (good...) conclusions might add up points in the end.*
Results	Available within two weeks from exam date (hopefully...)

Outline

1.CMOS, etc. (5 p).....2
2.Noise (5 p).....3

3.OP/OTA, Stability (5 p)....4
4.Gain stages, Speed, etc. (5 p)....5
5.Miscellaneous (5 p)....6

1. CMOS, ETC. (5 P)

Consider the circuit in Figure 1.1 below. An input signal is fed as a **current** at the primary side of a current mirror. The two transistors are equally large and have an aspect ratio of W/L. Let the input current be a ramp as a function of time.

1) What are the minimum and maximum input currents that you can apply to this circuit without saturating the output?

2) **Indicate the operating regions** for both transistors in the graph as the input current increases from minimum to maximum.

3) For which input current derivatives will you have a slew rate limitation due to the large capacitor C_L?

Make valid assumptions and motivate them well.

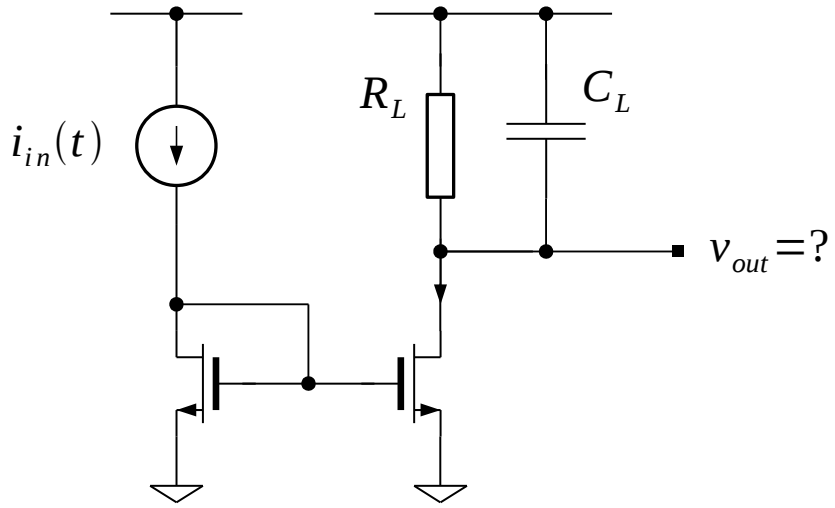

Figure 1.1: Current mirror with passive load.

- *This exercise will show that you have understood basic small-signal properties and the relations between them. Make valid assumptions and motivate them well.*
- *Sketch does not mean: draw with infinite accuracy, but maintain something realistic.*

2. NOISE (5 P)

✗ *We'll take a simple one this time too ...*

Consider the circuit in Figure 2.1. It is a you-know-what. The circuit is balanced symmetrically such that the input and output DC points are equal.

1) Derive a compact expression of the **total output noise power** for the circuit**!**

2) Derive the **input-referred noise spectral density!**

Make valid assumptions and motivate them well!

✗ ***Finding a compact expressions implies in this context: "Minimize the number of parameters in your expression."***

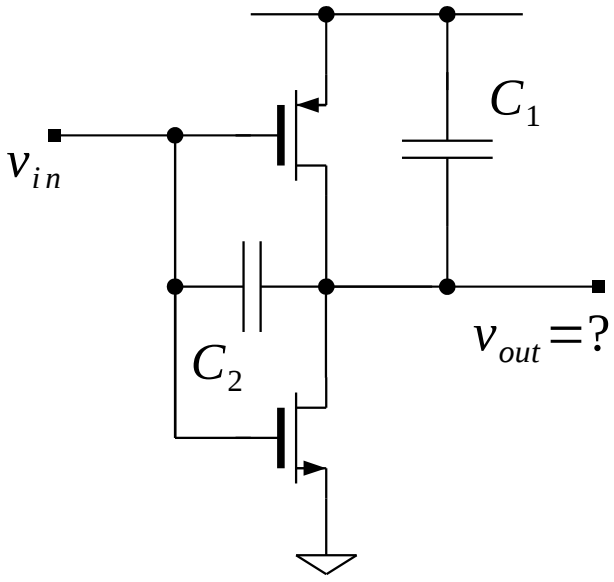

Figure 2.1: Phew! Three transistors...

✗ *Tip! Use symmetries to speed up your conclusions.*

✗ *Don't forget that you have to consider the **total noise power** at the output. Hint: use the noise brickwall bandwidth:* $p_1/4$ *(see for exampleJohns Martin).*

3. OP/OTA, STABILITY (5 P)

✗ *OK, so we saw this one last exam... but the number of answers was low... show me that you can plug in the numbers and understand the exercise.*

Consider the configuration in Figure 3.1, which consists of a current mirror and two other transistors. One can see that this is a simplified version of a current-mirror OTA. You can safely assume that all transistors operate in their saturation regions. Obviously it is a kind of two-stage amplifier (?) and you would have a parasitic capacitance, C_p, as indicated in the figure.

Assume the following: (1) $C_{gs} \approx C_{ox} W L/2$ is the dominating capacitor of a single NMOS transistor and for simplicity (2) $g_{mp} = g_{mn}$.

For which values of C_L does the circuit have a 63-degree phase margin (and more)? Especially, express how this relates to the mirror ratio, K.

Make valid assumptions and motivate them well!

✗ *Minimize the number of parameters in your expressions.*

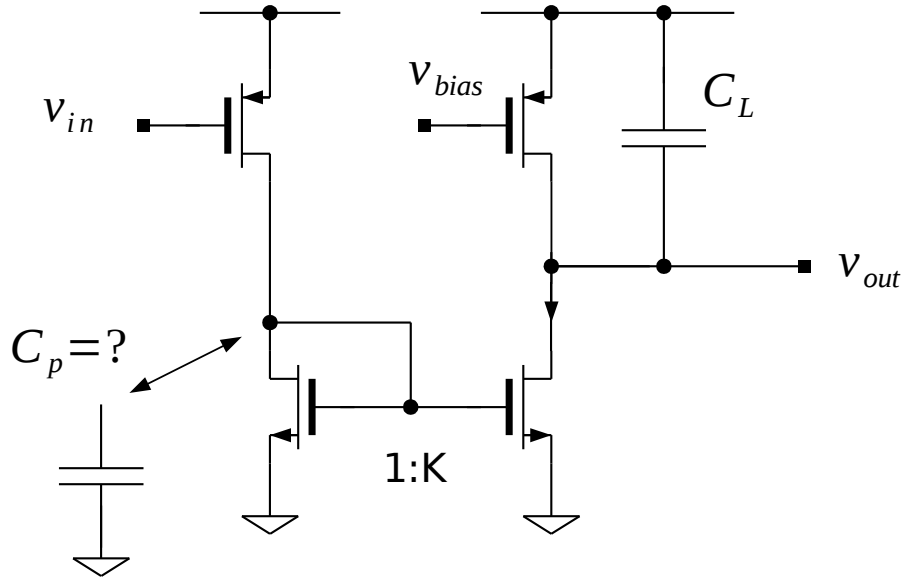

Figure 3.1: Transistors in a gain configuration.

✗ *Once again! Any (reasonable) try to answer the question can give you credits!*

✗ *And once again! Do not forget to present your results properly!*

✗ $\tan^{-1}(\text{large number}) \approx 90$ *degrees,* $\tan^{-1}(2) \approx 63$ *degrees.*

4. GAIN STAGES, SPEED, ETC. (5 P)

Consider the circuit in the figure below. An input signal is fed to the gate of the NMOS transistor. The DC output voltage, v_{out} - at the drain of the transistor - is fixed by a very, very, very, very large resistor, R_{set}. There is a capacitive load, C_L, between transistor drain and positive supply. The transistor operates in its saturation region. Further on, the input voltage is biased at

$$V_{IN}=V_{dd}/2 . \tag{4.1}$$

Now, assume that this amplifier has a certain slew rate of SR in its bias operating point. Sketch how the following parameters depend on slew rate if the **capacitance, C_L, is fixed**:

1) Transconductance g_m,
2) output conductance g_{ds},
3) DC gain $A_0=g_m/g_{ds}$,
4) dominant pole p_1, and
5) unity-gain frequency ω_u.

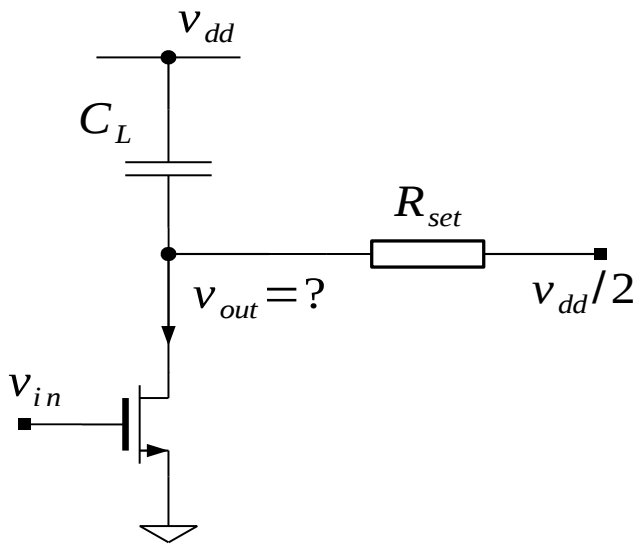

Figure 4.1: Common-something with some kind of load and stuff.

- *This exercise will show that you have understood basic small-signal properties and the relations between them. Make valid assumptions and motivate them well.*
- *Sketch is sketch.*
- *If capacitance is fixed, what does that imply on another important parameter (read current) for a given slew rate?*

5. MISCELLANEOUS (5 P)

> ✗ *Deliberately there are no pictures associated with these exercises. Fill in the gaps yourself if you want to... Draw a figure as you think it was explained and then solve accordingly. Do not forget to present your results well!*

Please find some various, miscellaneous questions covering the lecture material and quizzes:

5.1 Data converters (2 p)

Assume you implement an N-bit flash ADC for a 1-V range. Further on, assume that the area of a comparator is inversely proportional to the squared LSB voltage that it must be able to detect.

How does the **total area** of a flash ADC **scale with the number of bits** given a fixed, overall voltage range it should convert?

5.2 Performance measures (3 p)

We touched upon this one in one of the lectures: assume you have an output voltage from a common-source stage with passive load given by

$$V_{out}(t)=V_{DD}-R_L\cdot V_{eff}^2(t) \text{ where } V_{eff}=V_{DC}+v_a\cdot\sin(\omega t) \quad (5.1)$$

When is the distortion 60 dB?