TSEI09, Analog Integrated Circuits, 2011-03-16
Written exam, TEN1

Date and time	2011-03-16, 14.00 - 18.00
Location(s)	TER3 (25 copies printed)
Responsible teacher	J Jacob Wikner, jacwi50, +46-70-5915938
Aid	Any written and printed material, including books and old exams. Note! No pocket calculators, no laptops, no iPods, no telephones, no internet connection.
Instructions	A maximum of 25 points can be obtained from the written exam. Three points can be obtained from quizzes. In total: 10 points are required to pass, 15 for a grade four, and 20 for a grade five. *x Hint! **Be strategic** when you pick exercises to solve. You have five exercises in four hours and you could therefore spend some 45 minutes on each exercise. That leaves you 15 minutes to relax...* Note that a **good motivation to your answer** must be included in your solutions in order to obtain maximum number of points! With "motivation" mathematical derivations are understood (and not only text). Also note that the questions in this exam are divided into logical sections. You may use **Swedish, English or German** in your answers. Notice that some questions are **'hidden"in the text** and therefore: read the instructions carefully! *x Notice also that eventhough you do not fully know the answer, please add some elaborations on your reasoning around the question. Any (good...) conclusions might add up points in the end.*
Results	Available by 2011-03-31 (hopefully...)

Outline

1. CMOS, ETC. (5 P)

Consider the circuit in Figure 1.1 below. An input signal is fed as a **current** at the primary side of a current mirror. The two transistors are equally large and have an aspect ratio of W/L.

1) Sketch the **transimpedance of the circuit** (i.e., the output voltage as function of input current).

2) Clearly **indicate the operating regions** for both transistors in the graph. Use the following regions: linear, saturation, subthreshold, and cut-off.

3) What is the **maximum transimpedance** (i.e., "gain") you can obtain in this circuit? For which i_{in} does this happen?

Make valid assumptions and motivate them well.

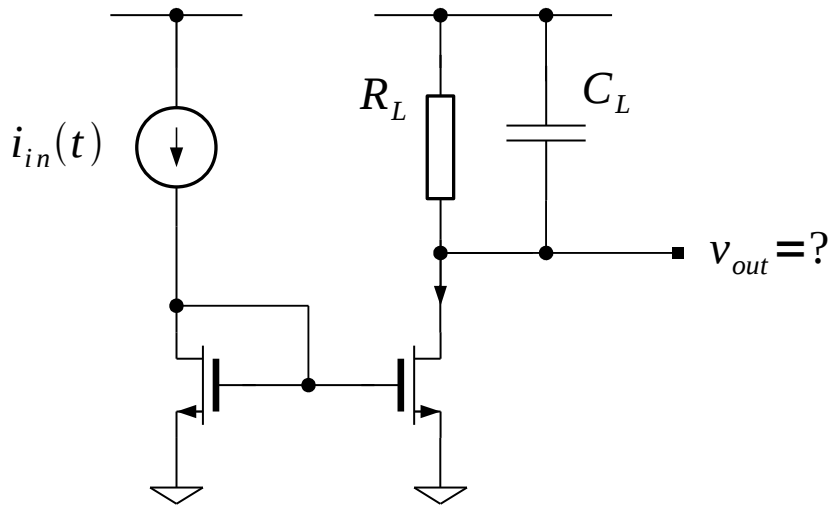

Figure 1.1: Current mirror with passive load.

- *This exercise will show that you have understood basic small-signal properties and the relations between them. Make valid assumptions and motivate them well.*
- *Sketch does not mean: draw with infinite accuracy, but maintain something realistic.*

Solutions

Hmm... this can probably not be easier... The output voltage is equal to:

$$v_{out}(t)=V_{DD}-R_L\cdot i_{in}(t) \tag{1.1}$$

If we assume the mirror does its job. Further on, the left-most transistors is always saturated "per definition". The right-most one will however run through three different regions: subthreshold, saturation, linear at last.

The maximum transimpedance is R_L (see formula above!!!) and it is found in the saturation region.

This is given by $V_{out}>V_{eff}$, i.e.,

$$V_{DD}-R_L\cdot I_d>V_{eff}=\sqrt{\frac{I_d}{\alpha}}\Rightarrow I_d+\sqrt{\frac{I_d}{\alpha\cdot R_L^2}}-\frac{V_{DD}}{R_L}<0 \tag{1.2}$$

from which we can find the current

$$\sqrt{I_d}=\frac{-1}{2R_L\sqrt{\alpha}}\pm\sqrt{\frac{1}{4R_L^2\alpha}+\frac{V_{DD}}{R_L}}=\frac{-1\pm\sqrt{1+4R_LV_{DD}\alpha}}{2R_L\sqrt{\alpha}} \tag{1.3}$$

which would give us

$$I_d<\left(\frac{-1\pm\sqrt{1+4R_LV_{DD}\alpha}}{2R_L\sqrt{\alpha}}\right)^2=\frac{1+2R_LV_{DD}\alpha\pm\sqrt{1+4R_LV_{DD}\alpha}}{2R_L^2\cdot\alpha} \tag{1.4}$$

or something like that... For the fun of it:

$$I_d<2\frac{V_{DD}}{R_L}\cdot\frac{1+\frac{1}{2}\cdot4R_LV_{DD}\alpha\pm\sqrt{1+4R_LV_{DD}\alpha}}{4R_LV_{DD}\alpha}=\frac{V_{DD}}{R_L/2}\cdot\frac{1+x/2\pm\sqrt{1+x}}{x} \tag{1.5}$$

The important thing is that you demonstrate that the limit can be calculated quite "easily".

2. NOISE (5 P)

> ✗ *NOTE! This exercise is fairly "simple", or at least straightforward this time. Present your solutions very clearly. Show all the steps and motivate well to get full points!!!*

Consider the circuit in Figure 2.1. The input voltage, v_{in}, is connected to the PMOS and the current mirror sets the bias current through the active device.

1) Derive a compact expression of the **total output noise power!**

2) Derive the **input-referred noise spectral density!**

3) Express and sketch **how the total output noise power depends on the bias current, I_0 !**

Only consider the thermal noise of the transistors. Make valid assumptions and motivate them well!

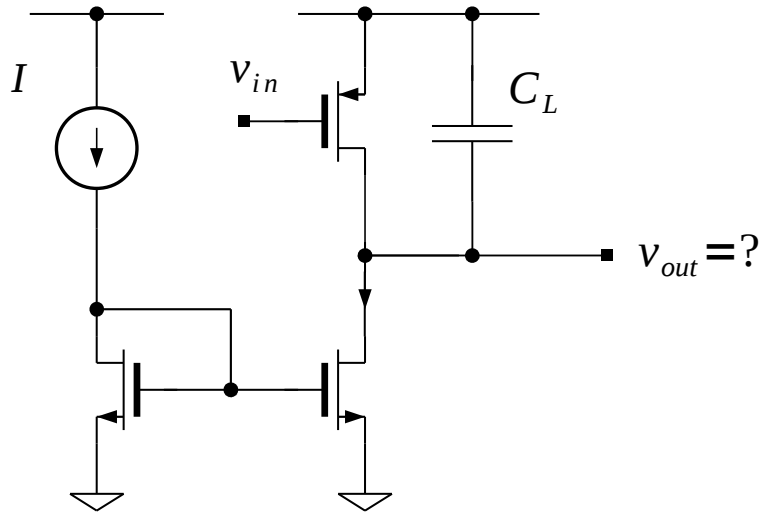

Figure 2.1: Phew! Three transistors...

> ✗ *Tip! Use symmetries to speed up your conclusions.*
>
> ✗ *Don't forget that you have to consider the **total noise power** at the output. Hint: use the noise brickwall bandwidth: $p_1/4$ (see for example Johns Martin).*

Solutions

See TSTE08 from same date.

3. OP/OTA, STABILITY (5 P)

OK, so a question on stability in amplifiers, etc. Consider the configuration in Figure 3.1, which consists of a current mirror and two other transistors. One can see that this is a simplified version of a current-mirror OTA. You can safely assume that all transistors operate in their saturation regions. Obviously it is a kind of two-stage amplifier (?) and you would have a parasitic capacitance, C_p, as indicated in the figure.

Assume the following: (1) $C_{gs} \approx C_{ox} W L/2$ is the dominating capacitor of a single NMOS transistor and for simplicity (2) $g_{mp} = 4 \cdot g_{mn}$.

For which values of C_L does the circuit have a 45-degree phase margin (and more)? Sketch how this relates on the mirror ratio.

Make valid assumptions and motivate them well!

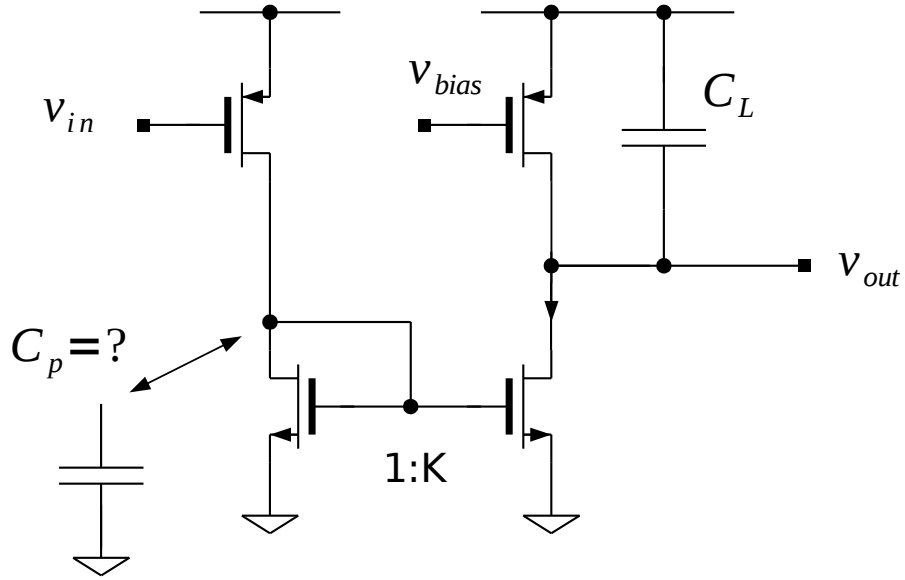

Figure 3.1: Transistors in a gain configuration.

- *Once again! Any (reasonable) try to answer the question can give you credits!*
- *And once again! Do not forget to present your results properly!*
- $\tan^{-1}(\text{large number}) \approx 90$ *degrees,* $\tan^{-1}(1) = 45$ *degrees.*
- *In the Bode plot: for each pole you pass, you drop 90 degrees.*
- *Hint! Assume the poles are well separated to simplify the maths!*
- *How large is* C_p *?*

Solutions

See TSTE08 from same date.

4. GAIN STAGES, SPEED, ETC. (5 P)

Consider the multi-stage comparator in Figure 4.1 below. It consists of N cascaded gain stages. All transistors operate in their saturation regions.

All the DC voltages are the same, i.e., at DC: $v_{in}=v_0=v_1=v_2=\ldots=v_N=v_{out}=V_{DD}/2.0$ they are all at half the supply voltage for maximum swing. Make life easy for yourself, assume $V_T=0$ too.

Assume the gate-source capacitance $\left(C_{gs}\approx C_{ox}WL/2\right)$ is dominating over other capacitors.

1) Find a compact expression on the **total DC gain** of the circuit.

2) Find a compact expression of the **total transition delay** through the circuit.

And don't forget the tips below... and make the assumptions you need.

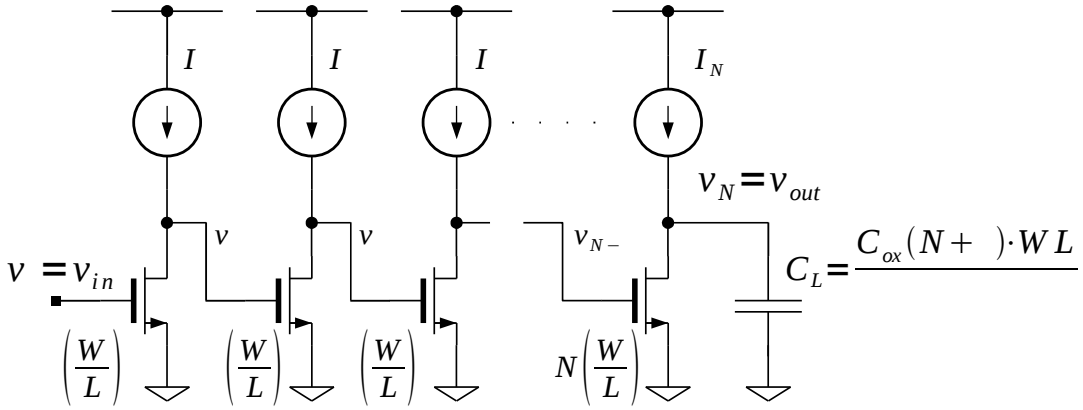

Figure 4.1: Some differential pair of some kind.

- *Finding a compact expressions implies in this context: "Minimize the number of parameters and express in terms of V_{DD}, N, and physical parameters."*
- *What is the relationship between the pole and the time constant of a circuit? Remember the lecture on comparators and speed!*
- *Since all DC voltages are equal, what does that imply on the currents for balancing the stages? Remember one of the quizzes!*
- *This exercises is easier than you think! Put at least some effort into it before you give up*

Solutions

We've seen it several times: the DC gain of a common-source is

$$A_0 = \frac{g_m}{g_{ds}} = \frac{2I_D/V_{eff}}{\lambda I_D} = \frac{2}{\lambda V_{eff}} \tag{4.1}$$

and exercise clearly states all DC levels are same. This means that the total gain must be just N times larger.

$$A_{tot} = \sum A_k = N \cdot A_0 = \frac{2N}{\lambda V_{eff}} = \frac{4N}{\lambda V_{DD}} = \frac{4NL}{\theta V_{DD}} \tag{4.2}$$

The pole of each state is given by its output impedance and the next-stage capacitance. We get:

$$p_k = \frac{g_k}{C_{k+1}} = \frac{\lambda I_d}{C_{ox}(k+1)WL/2} = \frac{\theta \mu_0 C_{ox} k (W/L) V_{eff}^2}{C_{ox}(k+1)WL^2/2} = \frac{2k\theta\mu_0 V_{eff}^2}{(k+1)L^3} = \frac{k\theta\mu_0 V_{DD}^2}{2(k+1)L^3} \tag{4.3}$$

The time constant is the inverse of that

$$\tau_k = \frac{1}{p_k} = \frac{2(k+1)\cdot L^3}{k\theta\mu_0 V_{DD}^2} \tag{4.4}$$

and the total delay is the sum of all τ_k and gives us

$$\tau_{tot} = \sum \tau_k = \frac{\sum 2(k+1)\cdot L^3}{k\theta\mu_0 V_{DD}^2} = \frac{2L^3}{\theta\mu_0 V_{DD}^2} \cdot \sum \frac{k+1}{k} = \frac{2L^3}{\theta\mu_0 V_{DD}^2} \cdot \left(N + \sum \frac{1}{k} \right) \tag{4.5}$$

5. MISCELLANEOUS (5 P)

> ✗ *Deliberately there are no pictures associated with these exercises. Fill in the gaps yourself if you want to... Draw a figure as you think it was explained and then solve accordingly. Do not forget to present your results well!*

Please find some various, miscellaneous questions covering the lecture material and quizzes:

5.1 Data converters (1 p)

Assume you implement an N-bit flash ADC for a 1-V range. Further on, assume that the area of a comparator is inversely proportional to the LSB voltage it needs to be able to detect.

How does the **total area** of a flash ADC **scale with the number of bits** given a fixed, overall voltage range it should convert?

5.2 Performance measures (2 p)

We touched upon this one in one of the lectures: assume you have an output voltage from a common-source stage with passive load given by

$$V_{out}(t)=V_{DD}-R_L\cdot V_{eff}^2(t) \text{ where } V_{eff}=V_{DC}+v_a\cdot\sin(\omega t) \quad (5.1)$$

Find a compact expression for the **spurious free dynamic range (SFDR)** at the output! Make valid assumptions and motivate them well. (If you do not know what SFDR is, pick some other clever performance measure...)

5.3 CMOS basics (bulk effects) (2 p)

> ✗ *This is for those who have studied a bit extra...*

Assume you implement a current source with PMOS transistors sourcing current from the positive supply (VDD). Now, we have two options: (1) connect the bulk of the cascode to either VDD or (2) to the node between the source and cascode transistor.

Elaborate on pros and cons with this approach. Refer to (a) bandwidth, (b) noise, (c) swing, and (d) output resistance (at DC).

Solutions

Number 1:

An N-bit flash requires 2^N comparators and the voltage step is $1/2^N$. The area is inversely dependent on the voltage step, i.e., $A \sim 1/(1/2^N) \sim 2^N$ for each comparator. In total, we have 2^N comparators, i.e., the overall ADC area scales with $2^N \cdot 2^N = 2^{2N}$.

Number 2:

$$V_{out}(t) = V_{DD} - R_L \cdot V_{eff}^2(t) \text{ where } V_{eff} = V_{DC} + v_a \cdot \sin(\omega t) \tag{5.2}$$

Gives

$$V_{out}(t) = V_{DD} - R_L \cdot (V_{DC} + v_a \cdot x)^2 = V_{DD} - R_L \cdot \left(V_{DC}^2 + 2 V_{DC} v_a \cdot x + v_a^2 \cdot x^2\right) \tag{5.3}$$

or

$$V_{out}(t) = V_{DD} - R_L \cdot (V_{DC} + v_a \cdot x)^2 = V_{DD} - R_L \cdot \left(V_{DC}^2 + 2 V_{DC} v_a \cdot x + v_a^2 \cdot x^2\right) \tag{5.4}$$

or

$$V_{out}(t) = V_{DD} - R_L \cdot V_{DC}^2 - 2 R_L V_{DC} v_a \cdot x - R_L \cdot v_a^2 \cdot x^2 \tag{5.5}$$

Where $x^2 = (1+y)/2$ such that

$$V_{out}(t) = V_{DD} - R_L \cdot V_{DC}^2 - 2 R_L V_{DC} v_a \cdot x - R_L \cdot v_a^2 \cdot (1+y)/2 \tag{5.6}$$

and

$$V_{out}(t) = V_{DD} - R_L \cdot V_{DC}^2 - R_L v_a^2/2 - 2 R_L V_{DC} v_a \cdot x - R_L \cdot v_a^2 \cdot y/2 \tag{5.7}$$

x is the main component, $x = \sin(\omega t)$ and y is the second harmonic $y = \cos(2\omega t)$. This gives us the harmonic distortion as

$$HD_2 = \left(\frac{2 R_L V_{DC} v_a}{R_L v_a^2/2}\right)^2 = \left(\frac{4 V_{DC}}{v_a}\right)^2 = 16 V_{DC}^2/v_a^2 \tag{5.8}$$

Since the second harmonic is the only distortion term, the $HD_2 = SFDR$.