TSEI05, Analog and Discrete-time Integrated Circuits, 2010-03-16 Solutions exam, TEN1

Date and time	2010-03-16, 8.00 - 12.00
Locations	U7 and U10
Responsible teacher	J Jacob Wikner, jacwi50, +46-70-5915938
Aid	**Any written and printed material, including books.** **Note! No pocket calculator, no laptops, no ipods, no telephones, no internet.**
Instructions	A maximum of 25 points can be obtained, 10 points are required to pass, 15 for a grade four, and 20 for a grade five. (Hint! **Be strategic** when you pick exercises to solve. You have five exercises in four hours and you could therefore spend some 45 minutes on each exercise. That leaves you 15 minutes to relax...) Note that a **good motivation to your answer** must be included in your solutions in order to obtain maximum number of points! With "motivation" mathematical derivations are understood (and not only text). Also note that the questions in this exam are divided into logical sections. You may use **Swedish, English or German** in your answers. Notice that some questions are **"hidden" in the text** and therefore: read the instructions carefully! *ˣ Notice also that eventhough you do not fully know the answer, please add some elaborations on your reasoning around the question. Any (good...) conclusions might add up points in the end.*
Results	Available by 2010-04-01 (hopefully...)

Outline

1. MISC 1: CMOS, PERFORMANCE, ETC. (5 P)

In saturation region the current is given by

$$I_D = \alpha \cdot V_{eff}^3 \cdot \left(1 + \lambda^2 \cdot V_{ds}^2\right), \text{ where } \alpha = \frac{\mu_0 C_{ox}}{2 V_0} \cdot \frac{W}{L}. \tag{1.1}$$

This transistor is saturated for $V_{eff} < V_{ds}$ and on for $V_{eff} > 0$.

Assume the linear region behaves as “usual”.

The transconductance can be derived as

$$g_m = \frac{d I_D}{d V_{eff}} = 3\alpha \cdot V_{eff}^2 \cdot \left(1 + \lambda^2 \cdot V_{ds}^2\right) = \frac{3 I_D}{V_{eff}} \tag{1.2}$$

or

$$g_m = \frac{d I_D}{d V_{eff}} = 3\alpha \cdot V_{eff}^2 \cdot \left(1 + \lambda^2 \cdot V_{ds}^2\right) \approx 3\alpha^{1/3} \cdot \underbrace{\alpha^{2/3} \cdot V_{eff}^2}_{\approx I_D^{2/3}} \approx 3\alpha^{1/3} I_D^{2/3} \tag{1.3}$$

The output impedance or the output conductance is given by

$$g_{ds} = \frac{d I_D}{d V_{ds}} = 2 \underbrace{\alpha \cdot V_{eff}^3}_{\approx I_D} \cdot \lambda^2 \cdot V_{ds} \approx 2\lambda^2 V_{ds} I_D \Rightarrow r_{ds} = \frac{1}{2\lambda^2 V_{ds} I_D} \tag{1.4}$$

The DC gain of the transistor is

$$\frac{g_m}{g_{ds}} = g_m \cdot r_{ds} = \frac{3\frac{I_D}{V_{eff}}}{2\lambda^2 V_{ds} I_D} = \frac{1.5}{\lambda^2 V_{eff} V_{ds}} \tag{1.5}$$

Previously we have seen a term like $1/\lambda V_{eff}$. Now notice that the gain is also dependent on the output operating point too.

Sketch the DC transfer curve. The output voltage is

$$\begin{aligned} v_{out} &= V_{DD} - R_L I_D = V_{DD} - R_L \alpha (V_{in} - V_T)^3 \cdot (1 + \lambda^2 v_{out}^2) \\ v_{out} &\approx V_{DD} - R_L \alpha (V_{in} - V_T)^3 \end{aligned} \tag{1.6}$$

We have three regions.

1) Cut-off, when $v_{in} < V_T$ which means no current, which means $v_{out} \approx V_{DD}$. Draw a vertical line to mark the region.

2) Linear region when $v_{in} - V_T < v_{out}$. Draw a diagonal line to mark the region.

3) Saturation region, $V_T < v_{in} < v_{out} + V_T$. Sketch the curve between. Just draw something with a cubic relationship between input and output.

What is the DC gain?

Assume that R_L is much smaller than r_{ds} and the gain must be

$$A_0 = g_m R_L = \frac{3 R_L I_D}{V_{eff}} = 3 \frac{V_{DD} - V_{OUT}}{V_{IN} - V_T} \tag{1.7}$$

2. GAIN STAGES (5 P)

Keyword here is that all transistors but M3 need to be in saturation region. Notice in the exercise also that ϕ_1 is set to high.

First of all conclude that this is a common-drain amplifier (with a PMOS input), ie., gain should be around one or so, and it should have a wide bandwidth. We should expect that the output voltage tracks the input voltage by some:

$$v_{out} = v_{in} + \underbrace{V_{Tp} + \Delta v_p}_{v_{sg,p}} \tag{2.1}$$

To find the swings vs regions start from the VDD. The maximum output voltage must be

$$v_{out,max} = V_{DD} - \Delta v_p - \Delta v_p - \Delta v_n - V_{Tn} \tag{2.2}$$

The minimum output voltage can be

$$v_{out,min} = \Delta v_p \tag{2.3}$$

We can deduce the range for the input voltage from these values:

$$v_{in,min} = v_{out,min} - V_{Tp} - \Delta v_p = \Delta v_p - V_{Tp} - \Delta v_p = -V_{Tp} \tag{2.4}$$

and

$$\begin{aligned} v_{in,max} &= v_{out,max} - V_{Tp} - \Delta v_p = \\ &= V_{DD} - 2\Delta v_p - \Delta v_n - V_{Tn} - V_{Tp} - \Delta v_p = \\ &= V_{DD} - 3\Delta v_p - \Delta v_n - V_{Tn} - V_{Tp} \end{aligned} \tag{2.5}$$

which kind of indicates quite some limitation upwards.

The bandwidth is found by studying the small-signal schematics. Notice that the current source is a cascoded current source, ie., high output impedance. The NMOS M2 will only add some resistance in series with the current source with very high output impedance. Ignore it in the small-signal schematics.

Set up the nodal equations for whatever is remaining:

$$\begin{aligned} -g_{mp}(v_x - v_{in}) + (0 - v_x)g_{dsp} + (v_{out} - v_x)G_{on} = 0 \Rightarrow \\ (g_{mp} + g_{dsp} + G_{on})v_x = v_{out}G_{on} + g_{mp}v_{in} \end{aligned} \tag{2.6}$$

$$(0 - v_{out})sC_L + (v_x - v_{out})G_{on} = 0 \Rightarrow v_x = v_{out}(sC_L/G_{on} + 1)$$

Combine

$$(g_{mp} + g_{dsp} + G_{on})(1 + sC_L/G_{on})v_{out} = v_{out}G_{on} + g_{mp}v_{in} \tag{2.7}$$

gives

$$v_{out}\left(sC_L+(g_{mp}+g_{dsp})(1+sC_L/G_{on})\right)=g_{mp}v_{in} \tag{2.8}$$

gives

$$\frac{v_{out}}{v_{in}}=\frac{g_{mp}}{sC_L+g_{mp}+g_{dsp}+s\dfrac{C_L\cdot(g_{mp}+g_{dsp})}{G_{on}}}=\frac{\dfrac{g_{mp}}{g_{mp}+g_{dsp}}}{1+sC_L\cdot\left(\dfrac{1}{g_{mp}+g_{dsp}}+\dfrac{1}{G_{on}}\right)} \tag{2.9}$$

or

$$\frac{v_{out}}{v_{in}}=\frac{\dfrac{g_{mp}}{g_{mp}+g_{dsp}}}{1+\dfrac{s}{\dfrac{(g_{mp}+g_{dsp})G_{on}}{(g_{mp}+g_{dsp}+G_{on})C_L}}} \tag{2.10}$$

We can do our standard approximations, since quite often $g_{dsp}\ll g_{mp}$:

$$\frac{v_{out}}{v_{in}}\approx\frac{\dfrac{g_{mp}}{g_{mp}}}{1+\dfrac{s}{\dfrac{(g_{mp})G_{on}}{(g_{mp}+G_{on})C_L}}}=\frac{1}{1+\dfrac{s}{\dfrac{g_{mp}G_{on}}{(g_{mp}+G_{on})C_L}}} \tag{2.11}$$

Then we can use the assumption from the exercise, saying that $G_{on}>g_{mp}$ which gives us

$$\frac{v_{out}}{v_{in}}\approx\frac{1}{1+\dfrac{s}{\dfrac{g_{mp}G_{on}}{G_{on}C_L}}}=\frac{1}{1+\dfrac{s}{g_{mp}/C_L}} \tag{2.12}$$

We identify the DC gain, $A_0=1$ and the dominant pole, i.e., the bandwidth as $p_1=g_{mp}/C_L$.

The DC gain is constant and its graph as function of I_0 becomes quite dull... The g_{mp} depends on the current as for example

$$g_{mp}\sim 2\sqrt{\alpha I_0} \tag{2.13}$$

So sketch something that decreases with the square root of the current.

3. NOISE (5 P)

This is a current mirror and there are several ways to solve the problem. First of all. Identify the symmetry: the noise from M2 will be as visible on the output as will the noise from M1. They both describe a common-source. What about M3? Well, it is a current mirror as said, and the input current must be mirrored to the output. The ratio is unity in this example.

So the noise in the left-most branch, on the M3 can be either modelled as a current source or a voltage source. Doesn't matter. We can quickly calculate the noise due to M3 on the source-gate voltage of M2 and M3:

$$v_{sg(3)} = v_{n3}\frac{g_{m3}}{g_{m3}+g_{ds3}} \approx v_{n3} \tag{3.1}$$

This means that the noise from M3 will be approximately equal to the noise from M2.

The transfer function from gate of M1 to output is

$$A_1(s) = \frac{g_{mn}}{g_{dsn}+g_{dsp}+sC_L} = \frac{g_{mn}/(g_{dsn}+g_{dsp})}{1+\dfrac{s}{(g_{dsp}+g_{dsn})/C_L}} = \frac{A_{0n}}{1+s/p_1} \tag{3.2}$$

and due to symmetry we must have from M2 (and thus from M3 too in this example) to output:

$$A_2(s) \approx A_3(s) = \frac{g_{mp}}{g_{dsn}+g_{dsp}+sC_L} = \frac{g_{mp}/(g_{dsn}+g_{dsp})}{1+\dfrac{s}{(g_{dsp}+g_{dsn})/C_L}} = \frac{A_{0p}}{1+s/p_1} \tag{3.3}$$

Use the superformula to derive the noise spectral density at output:

$$S_0(f) = S_3(f)\cdot\left|A_3(s)^2\right| + S_2(f)\cdot\left|A_2(s)^2\right| + S_1(f)\cdot\left|A_1(s)^2\right| \tag{3.4}$$

and we have

$$\left|A_1(s)^2\right| = \left|A_2(s)^2\right|\cdot\frac{A_{0n}^2}{A_{0p}^2} = \left|A_3(s)^2\right|\cdot\frac{A_{0n}^2}{A_{0p}^2} = \left|A_2(s)^2\right|\cdot\frac{g_{mn}^2}{g_{mp}^2} \tag{3.5}$$

Combining the expressions gives us the output noise spectral density.

$$S_0(f) = \left(\left(S_3(f)+S_2(f)\right)\cdot\frac{g_{mp}^2}{g_{mn}^2} + S_1(f)\right)\cdot\left|A_1(s)^2\right| \tag{3.6}$$

Before we move on, we can here put an expression on the input noise spectral density:

$$S_{in}(f)=\frac{S_0(f)}{|A_1(s)^2|}=\left(S_3(f)+S_2(f)\right)\cdot\frac{g_{mp}^2}{g_{mn}^2}+S_1(f) \tag{3.7}$$

Insert the expressions on noise (given in the exercise) in these two expressions and you have the answers.

$$S_0(f)=4kT\gamma\left(\frac{2}{g_{mp}}\cdot\frac{g_{mp}^2}{g_{mn}^2}+\frac{1}{g_{mn}}\right)\cdot\frac{g_{mn}^2/g_{out}^2}{1+\omega^2/p_1^2}=\frac{2g_{mp}+g_{mn}}{g_{out}^2}\cdot\frac{4kT\gamma}{1+\omega^2/p_1^2} \tag{3.8}$$

M3 and M2 are identical. The input-referred spectral density becomes

$$S_{in}(f)=4kT\gamma\cdot\left(\frac{2}{g_{mp}}\cdot\frac{g_{mp}^2}{g_{mn}^2}+\frac{1}{g_{mn}}\right)=4kT\gamma\cdot\frac{2g_{mp}+g_{mn}}{g_{mn}^2} \tag{3.9}$$

The total noise power on the output can be found as the spectral density DC gain value times the brickwall filter bandwidth as given in the exercise. This means that

$$P_n=S_0(0)\cdot\frac{p_1}{4}=\frac{2g_{mp}+g_{mn}}{g_{out}^2}\cdot\frac{4kT\gamma\cdot g_{out}}{4C_L}=\frac{2g_{mp}+g_{mn}}{g_{out}}\cdot\frac{kT}{C_L}\cdot\gamma \tag{3.10}$$

The signal power is given in the exercise and the amplitude we can set to V_a = V_DD/2, which means we have the SNR as

$$SNR=\frac{P_s}{P_n}=\frac{1}{8}\cdot\frac{V_{DD}^2}{\frac{2g_{mp}+g_{mn}}{g_{out}}\cdot\frac{kT}{C_L}}\cdot\gamma=\frac{V_{DD}^2\cdot\gamma}{8kT}\cdot\frac{C_L\cdot g_{out}}{2g_{mp}+g_{mn}} \tag{3.11}$$

Insert some intelligent expressions for g_{mp}, g_{mn}, and g_{out}:

$$SNR=\frac{V_{DD}^2\cdot\gamma}{8kT}\cdot C_L\cdot\frac{(\lambda_p+\lambda_n)I_D}{(4\sqrt{\alpha_p}+2\sqrt{\alpha_n})\sqrt{I_D}}=\frac{V_{DD}^2\cdot\gamma\cdot(\lambda_p+\lambda_n)}{16kT}\cdot C_L\cdot\frac{\sqrt{I_D}}{2\sqrt{\alpha_p}+\sqrt{\alpha_n}} \tag{3.12}$$

The SNR now depends on some different terms. The first part, we can assume to be untouchable. Then we have the C_L, the sizes, $\alpha\sim W$, and the current, I_D. So:

1) Maximize current

2) Maximize capacitance

3) Minimize transistor sizes

There are of-course some side effects due to this that gives us preference among these three, but that is not part of the exercise.

4. HIGH-GAIN STAGES (OP/OTA) (5 P)

You can create a low gain stage in several different ways. The exercise requires common-source, and we have several options. If we start with NMOS input transistor, it would be:

1) NMOS input with PMOS diode load

2) NMOS input with NMOS diode load

3) NMOS input with resistive load

4) NMOS input with floating NMOS load (essentially equal to case 2, but with V_{bias} something else than V_{DD})

Let's look at small-signal schematics first. The DC gain of the alternatives:

1) $A_0 = g_{mn1}/g_{mp2}$ and $p_1 = g_{mp2}/C_L$

2) $A_0 = g_{mn1}/g_{mn2}$ and $p_1 = g_{mn2}/C_L$

3) $A_0 = g_{mn1}\cdot R_L$ and $p_1 = 1/(R_L C_L)$

4) $A_0 = g_{mn1}/g_{mn2}$ and $p_1 = g_{mn2}/C_L$

For the DC operating point:

1)

$$V_{out} = V_{DD} - V_{Tp} - \Delta V_p = V_{DD} - V_{Tp} - \sqrt{\frac{I_D}{\alpha_P}} = V_{DD} - V_{TP} - (V_{in} - V_{Tn})\sqrt{\frac{\alpha_N}{\alpha_P}} \tag{4.1}$$

$$V_{out} = V_{DD} - V_{TP} - 2(V_{in} - V_{Tn})$$

since we know that $A_0 = g_{mn1}/g_{mp2} = \sqrt{\alpha_n/\alpha_p} = \sqrt{\mu_n/\mu_p}\cdot\sqrt{W_n/W_p} = 2$

2)

$$V_{out} = V_{DD} - V_{Tn} - \Delta V_n = V_{DD} - V_{Tn} - \sqrt{\frac{I_D}{\alpha_{N2}}} = V_{DD} - V_{Tn} - (V_{in} - V_{Tn})\sqrt{\frac{\alpha_{N2}}{\alpha_{N1}}} \tag{4.2}$$

$$V_{out} = V_{DD} - V_{Tn} - 2(V_{in} - V_{Tn}) = V_{DD} + V_{Tn} - 2V_{in}$$

since we know that $A_0 = g_{mn1}/g_{mn2} = \sqrt{\alpha_{n1}/\alpha_{n2}} = \sqrt{W_{n1}/W_{n2}} = 2$

3)

$$V_{out} = V_{DD} - R_L I_D = V_{DD} - R_L g_m \cdot \frac{V_{in} - V_{Tn}}{2} = V_{DD} - V_{in} + V_{Tn} \tag{4.3}$$

4)

$$\alpha_2\cdot(V_{bias2}-V_{out}-V_{Tn})^2=\alpha_1\cdot(V_{in}-V_{Tn})^2$$
$$V_{bias2}-V_{out}-V_{Tn}=\sqrt{\alpha_1/\alpha_2}\cdot(V_{in}-V_{Tn})=2(V_{in}-V_{Tn}) \quad (4.4)$$
$$V_{out}=V_{bias2}+V_{Tn}-2V_{in}$$

since we know that $A_0=g_{mn1}/g_{mn2}=\sqrt{\alpha_{n1}/\alpha_{n2}}=\sqrt{W_{n1}/W_{n2}}=2$

For 1), 2), 3) we do not need any bias. For 4) we need a current mirror.

Output swing

1) From ΔV_{n1} to $V_{DD}-V_{Tp}-\Delta V_{p2}$

2) From ΔV_{n1} to $V_{DD}-V_{Tn}-\Delta V_{n2}$

3) From ΔV_{n1} to V_{DD}

4) From ΔV_{n1} to $V_{bias}-V_{Tn}-\Delta V_{n2}$

Input swing (all stages are inverting - common-source -, use $v_{out}=\Delta v_n$ and solve for max case).

1) V_{Tn} to $V_{Tn}+(V_{DD}-V_{Tp}-\Delta V_n)/2$

2) V_{Tn} to $(V_{DD}+V_{Tn}-\Delta V_n)/2$

3) V_{Tn} to $(V_{DD}-V_{Tn}-\Delta V_n)/2$

4) V_{Tn} to $(V_{bias}+V_{Tn}-\Delta V_n)/2$

Difference between OTA and low-gain stage

1) Driving strength. Output drive current is decoupled from the input DC level. We can size regardless of input signal.

2) Common-mode rejection

3) Output range higher for operational amplifier. In our case the choice of

4) Area. OP amp is larger

5) Complexity and feedback is avoided

5. MISC 2: DATA CONVERTERS, TRANSMISSION LINES, IMPEDANCE MATCHING, ETC. (5 P)

5.1 Transmission Lines and Impedance Matching (2 p)

You want maximum power transfer (of signal power) from sender to receiver and you do not want any reflections or losses along the wire.

The drawbacks are area (more components) and power consumption (losses in termination due to DC currents).

5.2 Data Converters and Performance (3 p)

The speed of the first amplifier is given by

$$\tau_A = \frac{1}{p_1} = \frac{C_L}{g_{out}} = \frac{C_L}{g_{ds}} = \frac{C_L}{\lambda I_D} = \frac{C_L}{\lambda P_A / V_{DD}} = \frac{V_{DD} C_L}{\lambda P_A} \tag{5.1}$$

Sanity check: Higher C_L means longer delay. OK. Higher power means shorter delay, OK. Higher V_{DD} means longer delay (?), probably OK, we have higher swing to deal with.

The delay through the second amplifier is approximately

$$\tau_B = N \cdot \tau_0 = N \cdot \frac{V_{DD} C_L}{\lambda (P_B / N)} = N^2 \cdot \frac{V_{DD} C_L}{\lambda P_B} \tag{5.2}$$

where τ_0 is the delay of a single cell. Each stage consumes one Nth of the total P_B power. The ratio between the time constants is

$$\frac{\tau_A}{\tau_B} = \frac{\frac{V_{DD} C_L}{\lambda P_A}}{N^2 \cdot \frac{V_{DD} C_L}{\lambda P_B}} = \frac{1}{N^2} \cdot \frac{P_B}{P_A} \tag{5.3}$$

When is the right-most amplifier N times faster than the left one?

Compare the two time delays:

$$\tau_B = \frac{\tau_A}{N} \Rightarrow \frac{\tau_A}{\tau_B} = N \Rightarrow \frac{1}{N^2} \cdot \frac{P_B}{P_A} = N \Rightarrow P_B = P_A \cdot N^3 \text{ (!!!)} \tag{5.4}$$

So ... speed costs.