TSEI05, Analog and Discrete-time Integrated Circuits, 2010-03-16
Written exam, TEN1

Date and time	2010-03-16, 8.00 - 12.00
Locations	U7 and U10
Responsible teacher	J Jacob Wikner, jacwi50, +46-70-5915938
Aid	**Any written and printed material, including books.** **Note! No pocket calculator, no laptops, no ipods, no telephones, no internet.**
Instructions	A maximum of 25 points can be obtained, 10 points are required to pass, 15 for a grade four, and 20 for a grade five. (Hint! **Be strategic** when you pick exercises to solve. You have five exercises in four hours and you could therefore spend some 45 minutes on each exercise. That leaves you 15 minutes to relax...) Note that a **good motivation to your answer** must be included in your solutions in order to obtain maximum number of points! With "motivation" mathematical derivations are understood (and not only text). Also note that the questions in this exam are divided into logical sections. You may use **Swedish, English or German** in your answers. Notice that some questions are **"hidden" in the text** and therefore: read the instructions carefully! ˣ *Notice also that eventhough you do not fully know the answer, please add some elaborations on your reasoning around the question. Any (good...) conclusions might add up points in the end.*
Results	Available by 2010-04-01 (hopefully...)

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1. MISC 1: CMOS, PERFORMANCE, ETC. (5 P)

You just graduated from the University and has got your first employment. Your task is to implement an analog circuits using new CMOS building blocks.

The strange thing with the technology provided is that in the saturation region the current of the transistor is now given by:

$$I_D=\alpha\cdot V_{eff}^3\cdot\left(1+\lambda^2\cdot V_{ds}^2\right), \text{ where } \alpha=\frac{\mu_0 C_{ox}}{2V_0}\cdot\frac{W}{L}. \quad (1.1)$$

$V_{eff}=V_{gs}-V_t$ and $\lambda\cdot V_{ds}<1$ are the "normal" definitions, but the parameter V_0 is added to compensate for the cube of V_{eff}. This transistor is in its saturation region as long as $V_{eff}<V_{ds}$ and is on as long as $V_{eff}>0$. Assume the linear region behaves as "usual".

Elaborate on the characteristics of transconductance (g_m), gain $(A_0=g_m/g_{ds})$ and output impedance $(r_{out}=1/g_{ds})$ for this type of transistor. **Derive these parameters and express them using compact formulae suitable for hand calculations!**

Sketch the DC transfer curve for this type of NMOS transistor used in a common-source amplifier with resistive load towards the positive supply (see Figure 1.1). Indicate the transistor operating regions in your graph and the break points by **referring to the parameters you just derived**.

What is the DC gain?

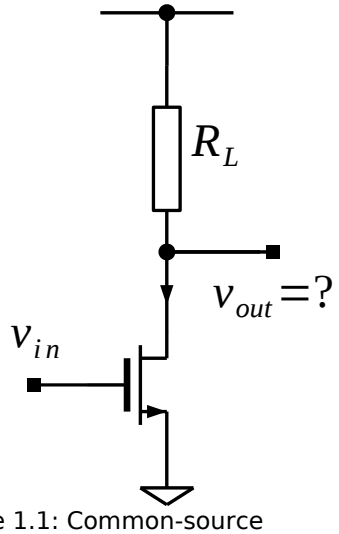

Figure 1.1: Common-source

- *This exercise will show that you have understood basic small-signal properties and desirable features of a transistor.*
- *Tip: It always helps with some figures for the small signal schematics too.*

2. GAIN STAGES (5 P)

Consider the circuit in Figure 2.1 which shows some strange (?) circuit driven by a cascoded current source. You can assume that the reference current, I_0, is generated by a wide swing current mirror hence the two additional transistors illustrated in the figure. The ϕ_1 and $\check{\phi}_1$ are two non overlapping switching phases.

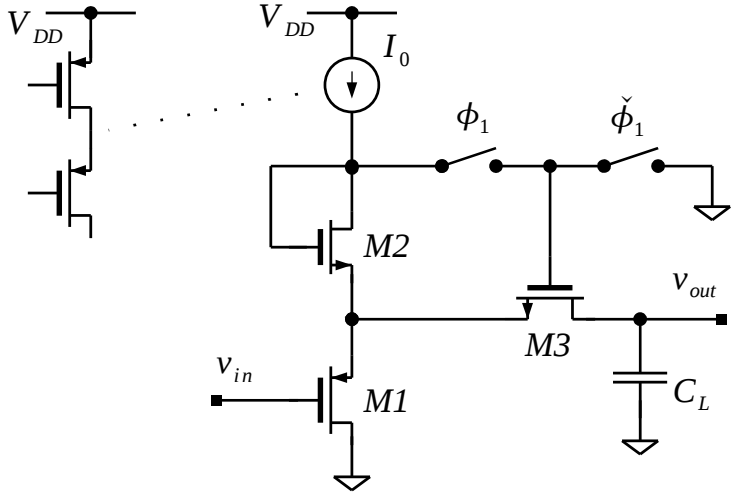

Figure 2.1: A circuit.

Determine the input and output range of the circuit that guarantees all transistors but M3 to be operating in the saturation region (don't forget to include the ones in the current source - assume wide-swing mirror). Assume that ϕ_1 is high and than $\check{\phi}_1$ is low. (In this phase, the ground is not connected to the gate of transistor M3). For the linear region, the current through M3 is given by:

$$I_D = \alpha_3 \cdot \left(2 V_{eff} V_{ds} - V_{ds}^2\right) \tag{2.1}$$

which can be used to calculate the on resistance of M3.

Sketch a diagram that shows the bandwidth and DC gain of the transfer function from v_{in} to v_{out} as a function of the current I_0. Indicate levels, break points, etc., in the graph and relate these to valid parameters. Assume that the conductance of the switch, G_{on}, is higher than the g_m of e.g. M1 and M2.

- *This exercise will show that you have understood the relation between schematics and small-signal expressions as well as large-signal operation.*
- *Don't forget to sanity check your results! Hint: what kind of gain stage is*

this?

✗ *Tip: Make a clever assumption when you calculate the output impedance to speed up your solution!*

3. NOISE (5 P)

Consider the circuit in Figure 3.1. It is a hmmm-hmm-hmm stage consisting of a hmm-hmmm mirror. Assume that the mirror ratio is 1 to 1, i.e., M2 and M3 are of same size. Also assume all transistors are operating in their saturation region.

All transistors are noisy, but we limit this exercise to only consider their thermal noise. So, you have in total **three** noise sources in this small circuit.

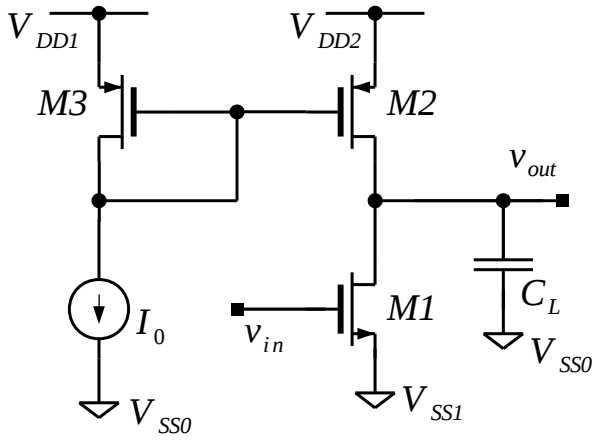

Figure 3.1: A simple (?) circuit.

Calculate the output- and input-referred noise spectral densities (use the symmetries in the circuit to speed up your calculations!!!). Equivalent input noise of the transistors is given by

$$v_n^2(f)=\frac{4kT\gamma}{g_m} \tag{3.1}$$

Elaborate on how you could maximize the signal-to-noise power ratio (SNR) at the output if a sinusoid at a frequency within the bandwidth is applied at the input! Assume that the **output** signal can swing from ground to supply, i.e., disregard the fact that the transistors have to be saturated for a short moment in your life. The signal power of a sinusoid is given by

$P_s=\frac{V_a^2}{2}$, where V_a is the amplitude of the signal. (3.2)

- *Tip: Parts of this exercise is found in the course exercise manual!*
- *Tip: To find max SNR, minimize the expression w.r.t. the number of parameters.*

✗ *Don't forget that you have to consider the **total noise power** at the output. Hint: use the noise brickwall bandwidth:* $p_1/4$ *(see Johns Martin).*

4. HIGH-GAIN STAGES (OP/OTA) (5 P)

Normally we want really high gain in our amplifiers, but now I want to ask you: “why?”

For example, assume you want a closed-loop gain of two, $A_{CL}=2$, you could (ignore the inversion for now) connect two resistors in a feedback configuration as shown in Figure 4.1 with a a two-stage amplifier as shown in the same figure and with $R_0=2R_1$. **But ...**

First, present and motivate a circuit solution for an open-loop, single-stage common-source amplifier with a small-signal gain of $A_0=2$. With “motivate” we understand that you must clarify the relationship between **transistor sizes, currents, gain, input- and output swing and DC operating points**.

> ✗ *Tip! Low-gain stages quite often form strict relationships between transistor sizes that can be used to derive the other parameters! Write down all relations you can identify.*

You also need to describe how any bias (if required) is generated for the circuit and this bias current relates to the other transistor sizes.

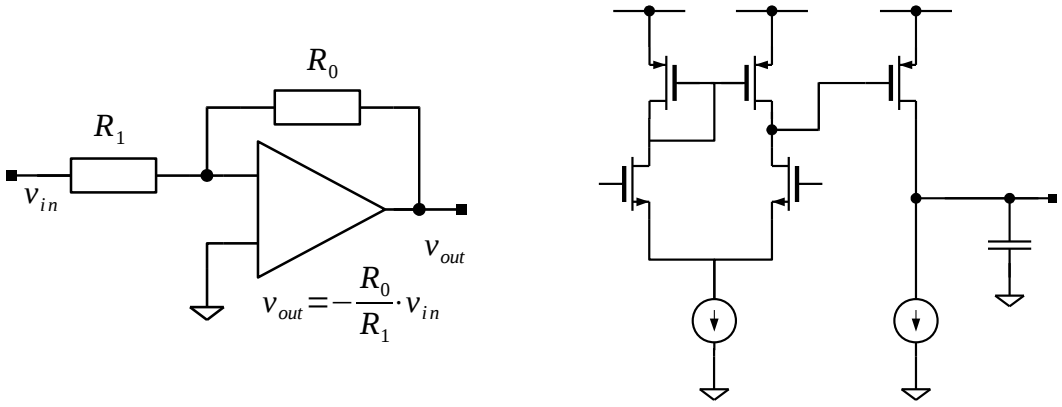

Figure 4.1: Closed-loop gain configuration and a two-stage amplifier.

Secondly, pick one example of a difference between open-loop and closed-loop amplifiers **with same overall gain**. **Highlight if the difference is beneficial or not for the respective amplifier.** You can touch upon **for example:** input and output range (IR, CMR, OR), speed (p_1, ω_{ug}), gain (A_0 vs A_{CL}), sensitivity (mismatch, PSRR), driving capability (I, SR), linearity (THD), noise, etc.

> ✗ *Don't just answer: SR is higher for amplifier B. Motivate why!!!*

- *In short: show that you have understood the fundamental basics of analog building blocks and that you can design a block from scratch!*
- *Once again! Any (reasonable) try to answer the question can give you credits!*

5. MISC 2: DATA CONVERTERS, TRANSMISSION LINES, IMPEDANCE MATCHING, ETC. (5 P)

Whew! Finally... the last question (this time...)

5.1 Transmission Lines and Impedance Matching (2 p)

OK, wake up! **Give two reasons** why you want to match the impedance levels of an electronic circuit! Show a couple of “self-explanatory” drawings.

What are the **drawbacks** using impedance matching networks?

5.2 Data Converters and Performance (3 p)

To achieve high-speed in a comparator you quite often cascade several stages and you do not really care about multiple poles since you do not feed back the signal.

Compare a single-stage with a multi-stage amplifier as shown in Figure 5.1. Assume **all** substages have the **same capacitive load** dominated by gate capacitance. This implies that the two capacitor elements shown in the figure are of same size as a gate capacitance of $C_L=2W_N LC_{ox}/3$ where W_N is the width of the transistors in the multi-stage architecture. All transistors have same channel length modulation and they have minimum length, L. The current sources are ideal, and their currents are parameters in your design.

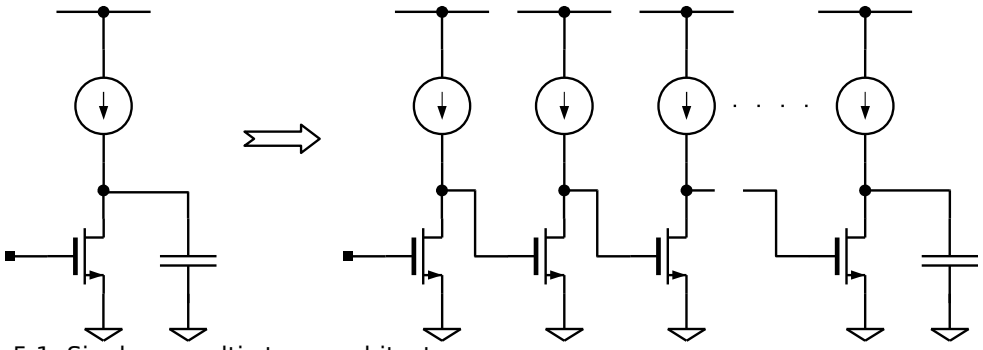

Figure 5.1: Single vs multi-stage architecture

Compare the speed of the two amplifiers (e.g. A and B) and **relate to the power**! This means: **express the ratio between the time constants**, τ_A/τ_B as a function of P_A and P_B (and other parameters, of course). The right-most amplifier in Figure 5.1 consists of N stages.

When is the right-most amplifier N times faster than the left one?

✗ *Tip: The exercise is not as difficult as it first appears to be! Use the standard*

formulas for A_0, p_1, ω_{ug}, as we have been doing so many times throughout the course. Make intelligent (if required) assumptions to solve it!