Linköpings universitet

Reinventing research and education

Analoga konstruktion, fortsättningskurs

J Jacob Wikner

Elektroniska kretsar och system

ISY

LiU EXPANDING REALITY

Föreläsning 1, Introduktion

Kursstart, grundläggande CMOS

LiU EXPANDING REALITY

Analoga konstruktion, fortsättningskurs

Vad innebär "analoga"?

Vad innebär integrerade kretsar?

Vad innebär fortsättningskurs?

Vad innebär kortnivå? Kretsnivå?

Webbresurser

WWW: http://www.isy.liu.se/edu/kurs/TSEI12

Blog: http://mixedsignal.wordpress.com

FB: http://www.facebook.com/mixedsignal

Studiehandboken 1

Prel. scheduled hours: 48
Rec. self-study hours: 112

Area of Education: Technology

Main field of studies: Electrical Engineering

Advancement level (G1, G2, A): G2

Aim:
The purpose is to give

- basic knowledge in analysis and design of analog and discrete-time circuits connected on a circuit board
- to give knowledge about different types of A/D- and D/A-converters and their usage
- to give knowledge about interconnects, termination of wires and load, dimensioning of circuits
- to give knowledge about noise and distortion

After the student has passed the course the student should be able to:

- Describe CMOS-transistors in different operation modes
- Describe the relationship between different design parameters and performance metrics
- Analyze amplifiers from small- and large-signal points of view
- Determine different types of performance measures for analog circuits

Studiehandboken 2

- Describe different methods for terminating wires/connecting chips
- Describe different types of noise and distortion, and also determine different type of noise- and distortion metrics.

Prerequisites: (valid for students admitted to programmes within which the course is offered)
Knowledge of basics in circuit theory, linear systems, and electronics.

Note: Admission requirements for non-programme students usually also include admission requirements for the programme and threshhold requirements for progression within the programme, or corresponding.

Organisation:
The course has lectures, lessons, and computer-based group exercises.

Course contents:
Introduction to CMOS technology: Integrated circuit components, such as PMOS and NMOS transistors, capacitors. Analyze one-stage amplifiers and operational amplifiers from a small

Studiehandboken 3

Course contents:

Introduction to CMOS technology: Integrated circuit components, such as PMOS and NMOS transistors, capacitors. Analyze one-stage amplifiers and operational amplifiers from a small signal point of view as well as from a large signal point of view. Determine different types of performance measures for differential amplifiers. D/A-converters: Different types, transfer functions, determine of output signal, offset errors. A/D-converters: Different types, quantization errors, comparators, resolution. Termination of wires: different techniques, high frequency systems, reflection. Noise: Different types, spectral density, noise bandwidth, models and metrics of noise, noise in devices. Distortion: Quantization, aliasing, bandwidth, and harmonic distortion.

Course literature:

For the first lectures material will be distributed and in addition, the literature will be given on the course homepage before start.

Examination:

A written examination	4,5 ECTS
Laboratory work	1,5 ECTS

Written exam (TEN1) During the lectures five quizzes will be handed out. The answers will be returned during the same lecture. Out of five quizzes one can maximally obtain three points. These points can be accounted for in the written exam. The written exams contains of five exercises totalling 25 points. With correct quizzes, the student can obtain a total of 28 points. The grading is: 10p: 3, 15p: 4, 20p: 5.

Kort kurshistorik 1

Kursen har funnits sedan 1980-talet

- Utvecklas hela tiden (elektronik ...)
- Vi pendlar lite fram och tillbaka mellan IC och PCB

Nytt i år

- Utökat lektionsmaterial
- Fortsatta föreläsningar på svenska

Analoga konstruktion, fortsättningskurs

J Jacob Wikner (Allt)

Tekn. Dr., Linköpings universitet 2001

Ericsson, Imperial College, Infineon, Sicon, AnaCatum, Cognicatus, LiU, Sick-IVP, SAAB

Docent 2014

Vad är analogt - inte bara spänning och ström

Det handlar om avvägningar (trade-offs)

Målen är inte lika "ortogonala" som i digital konstruktion

Det finns inga bra verktyg för att hantera avvägningar

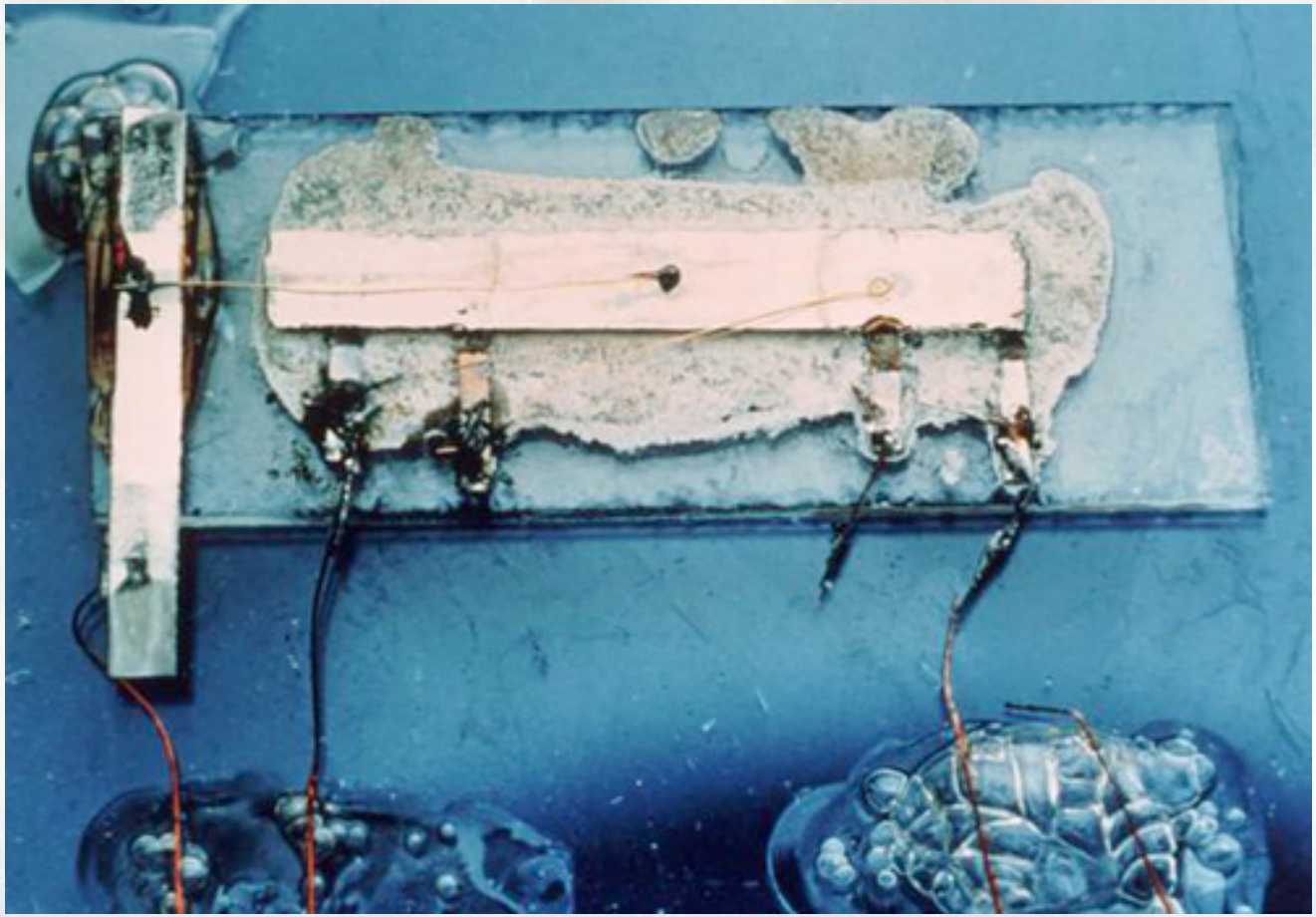
Det finns ingen automatiserad syntes

Det finns ingen direkt portning mellan processer/geometrier

Guru-kunskap!

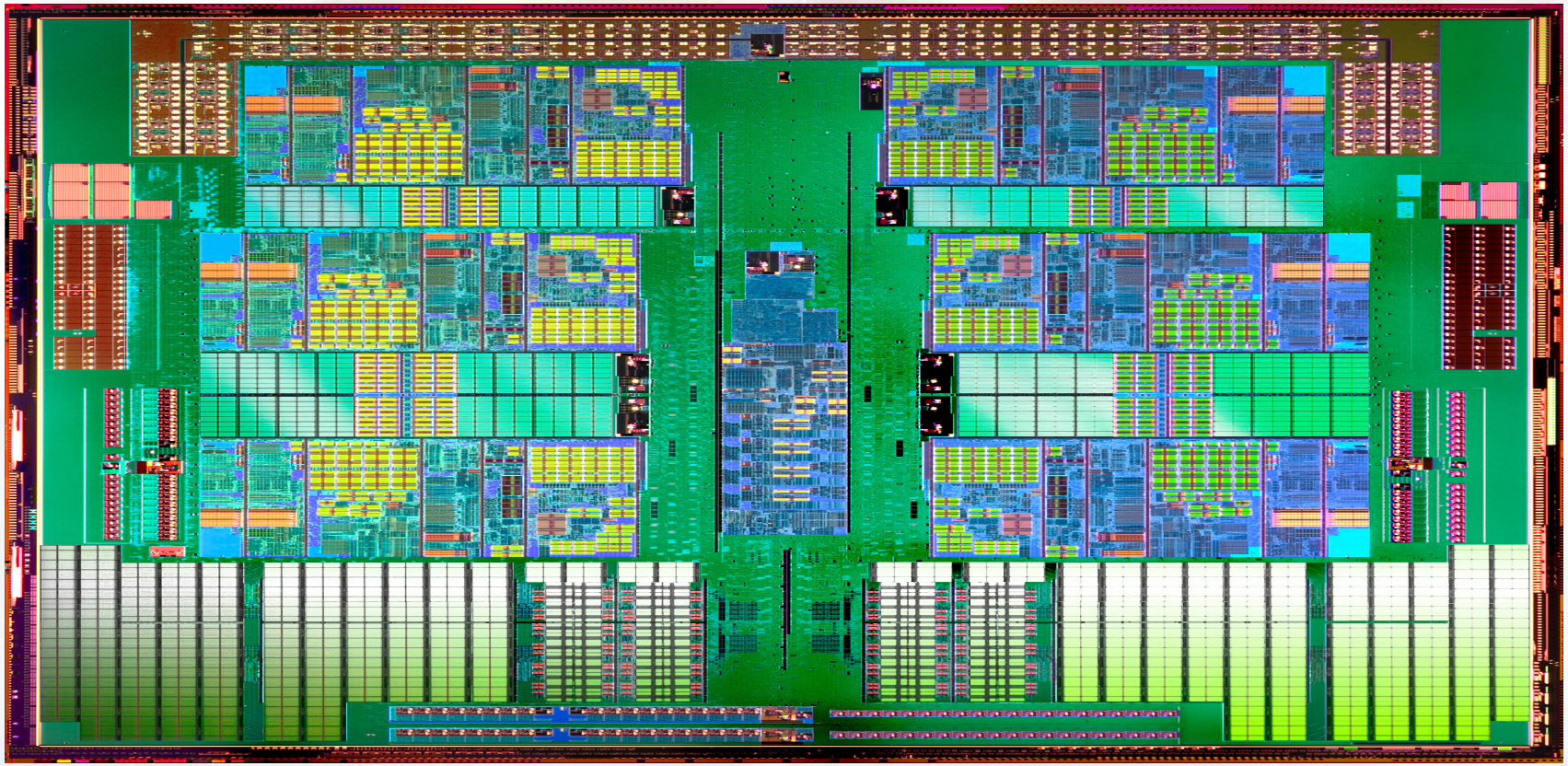
Vad är en integrerad krets? @1947

Vad är en integrerad krets? @1959



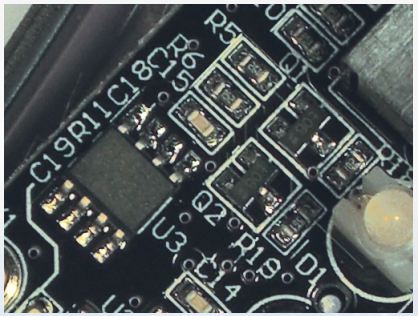
Courtesy of Texas Instruments

Vad är en integrerad krets? @2010



Courtesy of Advanced Micro Devices, Inc. (AMD) (Stretched picture)

Vad är ett kretskort?



http://en.wikipedia.org/wiki/GNU_Free_Documentation_License

Vad är en integrerad krets? @future

"Allt" kommer till slut sitta i samma förpackning

RF, digitalt, analogt, mixed-signal

Kommunikationsgränssnitt

http://en.wikipedia.org/wiki/GNU_Free_Documentation_License

En historielektion

Jämför med Moores lag

Skalar analogt?

Vad är begränsningen?

A brief history of time ...

Kursinnehåll

Lektionerna följer föreläsningarna

Tre laborationsmoment a fyra timmar (simulator)

Kanske mjukvarustyrda lektioner - beror lite grann på

2 x 2 timmar

Tentamen

Skriftlig examen, "open-book"

Quizzar, "tre av fem"

Föreläsningarna

#	Analoga konstruktion, fortsättningskurs
1	**Introduktion, kursupplägg, information, motivering CMOS-transistorn, grundläggande, kretskort vs. Kisel.** Hur ser det typiskt ut på insidan av ett kiselchip. Vilka byggstenar finns det och vad jobbar vi i för typ av omgivning.
2	**Analoga kretsar 1. Enkla byggstenar, karaktäristik. Pol-förstärkningsavvägning.** Vi börjar med att titta på de mest grundläggande kretsarna som typiskt används: common-source, common-gate, common-gain, inverterare, buffer, med flera. Vi kommer se hur så kallad enstegsförstärkare beter sig.

#	Analoga konstruktion, fortsättningskurs
3	**Analoga kretsar 2. Fler kretsar på kiselnivå. Mer om förstärkaren.** I vissa tillämpningar måste man ha t.ex. höghastighetsförstärkare, eller förstärkare med hög förstärkning, och dessa konstrueras på speciella sätt. Hur ska vi tänka när vi sätter samman dessa. När vi tittar i datablad - vilken förstärkare ska vi använda oss av?
4	**Förstärkaren, stabilitet och kompensering** Mer om stabilisering och varför man behöver stabilisera en förstärkare. Poler, insvängningsförlopp, med mera.

#	Analoga konstruktion, fortsättningskurs
5	**Brus och prestandamått.** Hur korrekt är "bra" och hur gör man något ännu mer noggrannt? Vi tittar på prestandamått såsom SFDR, SNDR, THD, MTPR, med flera. Vi måste också titta på hur vi beräknar brus i olika tillämpningar. När vi hittar en brussiffra i ett datablad - vad betyder det? Hur modellerar man bruset i en förstärkare.
6	**Dataomvandlare och filter** För att konditionera våra signaler och föra dem mellan olika domänener behöver vi typiskt filter och dataomvandlare. Vi kommer titta på nomneklaturen för olika typer av dataomvandlare, varför vissa ser ut som de gör och varför de inte går att använda eller varför man skulle välja just en typ.

#	Analoga konstruktion, fortsättningskurs
7	**"PCB vs. Kisel", dvs vågledare och terminering och signaltyper.** Vad är ett kretskort och vad skiljer det från en kiselflisa. Hur ser de olika komponenterna ut i det här fallet. Vi kommer titta på vågledarekvationerna för att förstå hur signaler (spänning/ström) breder ut sig på kretskort och hur man kan förbättra situationen för dem.
8	**Matning och referens (avkopplingskondensatorer)** På ett kretskort måste vi vara försiktiga med hur matningar distribueras mellan olika komponenter, såsom regulatorer, mottagarchip, med mera. Hur ska vi kunna garantera att den här matningen får en bra frekvensgång, dvs är stabil för "alla" frekvenser och "alla" störningar?

#	Analoga konstruktion, fortsättningskurs
9	**Klockning, timing, med mera** I den blandade domänen (digitalt/analog) - hur kan vi klocka olika chip och veta att signaler når dit de ska i tid? Vad händer t.ex. om vi antar linjär settling, vågledarreflektion, med mera, såsom vi har tittat på det tidigare i kursen. Hur ska man tänka? Vi tittar på byggblock såsom PLL och DLL som kan användas för ytterligare kontroll över timing.
10	**Diverse och sammanfattning, med mera** Sammanfattning av kursen, en liten utsikt över fler block ni kommer stöta på: regulatorer, skyddsdioder (ESD), med mera.

Laborationer

Tre mjukvarulabbar (obligatorisk närvaro)

1. CMOS-förstärkare
2. Avkopplingskondensatorer
3. Terminering och transmissionsledningar

Datorstödda lektioner (mot slutet av kursen, på begäran)

Allmänna frågeställningar, uppgifter från häftet

Tentamen

"Open-book"

Allt material kan tas med till tentamen.

Inte miniräknare.

Fem uppgifter, fem poäng vardera

Var strategisk!

Quizzes, snabbfrågor

Fem “slumpmässiga” frågor delas ut

En poäng ges på varje om rätt svar

Maximalt tre poäng kan ni tillgodoräkna er på skriftlig examen

Gäller för ett år (tre examinationstillfällen)

Ni får återkoppling direkt

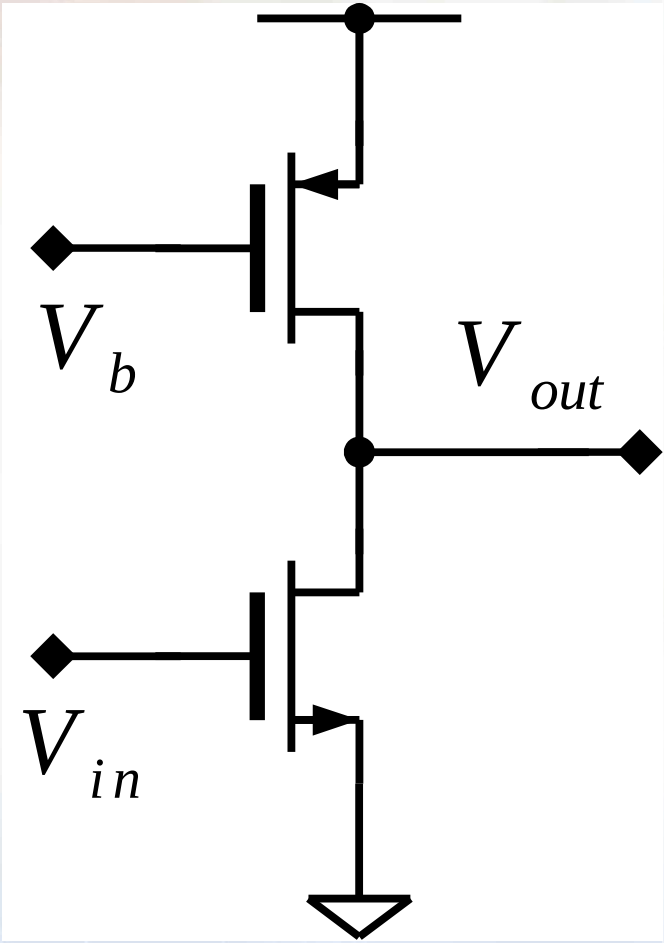
Exempel: Quiz (ges på engelska)

In a common-source amplifier, to minimize the output-referred noise, how should you design the transconductance of the active load?

1) To be as high as possible

2) To be as low as possible

3) The active load does not add noise to the output



Litteratur

Analoga kretsar, Bengt Molin

High Speed Digital Design: A Handbook of Black Magic, Johnson and Graham

Analog Integrated Circuit Design, Johns and Martin

Signal and Power Integrity - Simplified, Bogatin

Utdelat material via webben ...

... och du måste förstås leta själv

Allmän motivering: Varför analog konstruktion?

Gränssnittet till den riktiga världen

Integration av många komponenter på SOC

Men: försök gå till digitalt så snart du kan i signalkedjan

Dataomvandlare är gränssnittet (vem konstruerar dem?)

Integrera så snart du kan

Möjligheterna är mycket större. Även analoga kretsar är programmerbara.

Vart kan det här bära?

Linköping master thesis at the CES 2012 (Las Vegas)

Linköping master thesis at the CES 2014 (Las Vegas)

Fingerprints strikes a deal with Tier 1

Signal Processing Devices AB

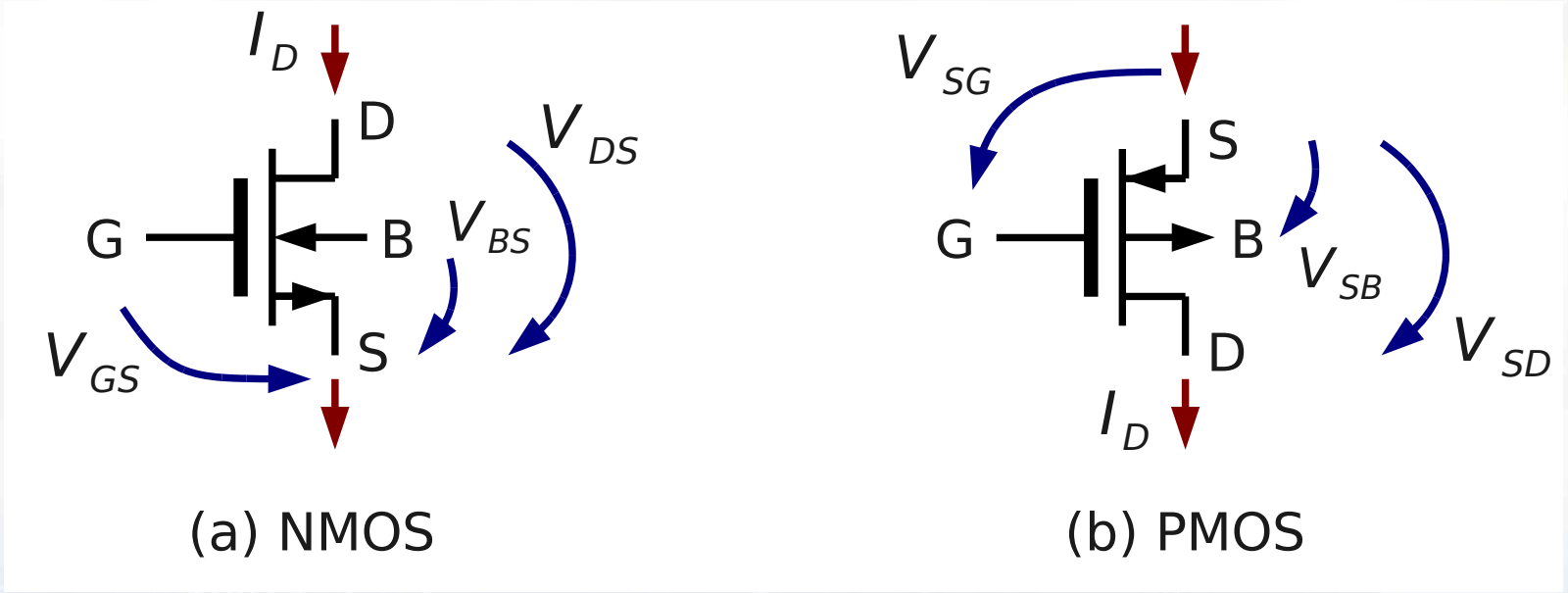
AnaCatum Design AB

Zzzzzzz, zzzz - kom till saken!

MOS-transistorn

... jag hatar fysiken bakom ...

för mej är det bara ett par symboler med lite formler...



(a) NMOS (b) PMOS

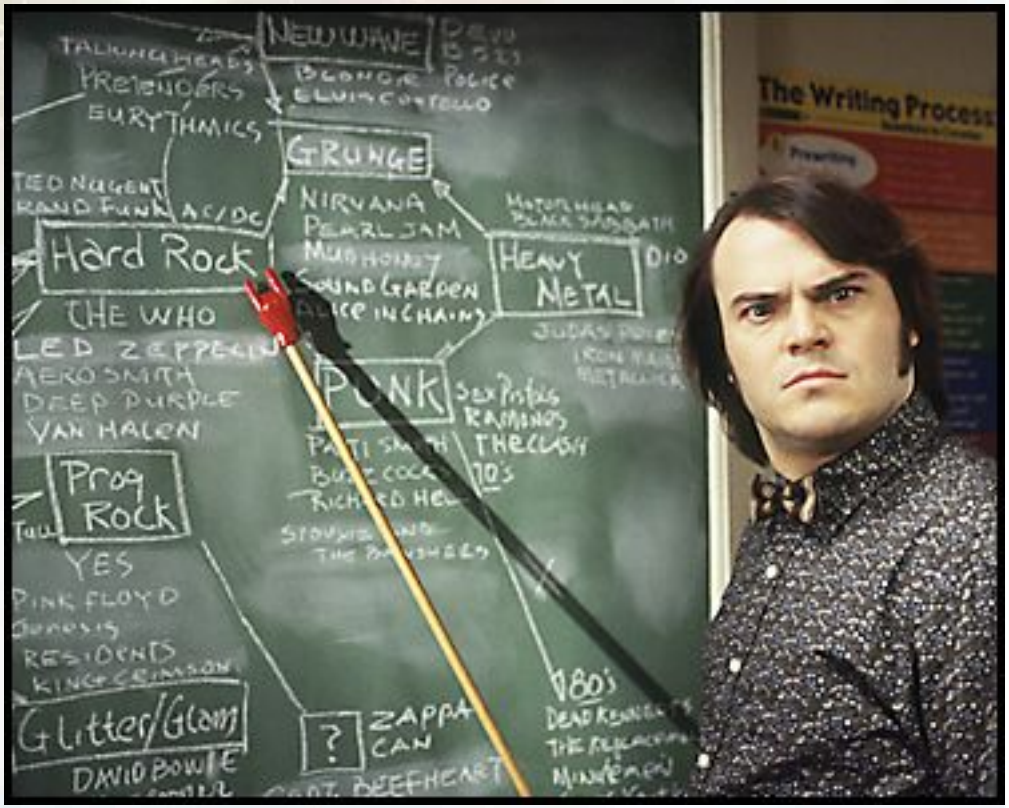
Fysiska aspekter

Arbetsområden

Mättad, linjär, av

Kapacitiv effekt

etc, etc



Arbetsområden

Subthreshold (cut-off)

$$I \approx 0$$

$$V_{eff} < 0$$

Linear (low gain)

$$I \approx \alpha \cdot \left(2 V_{eff} V_{ds} - V_{ds}^2 \right)$$

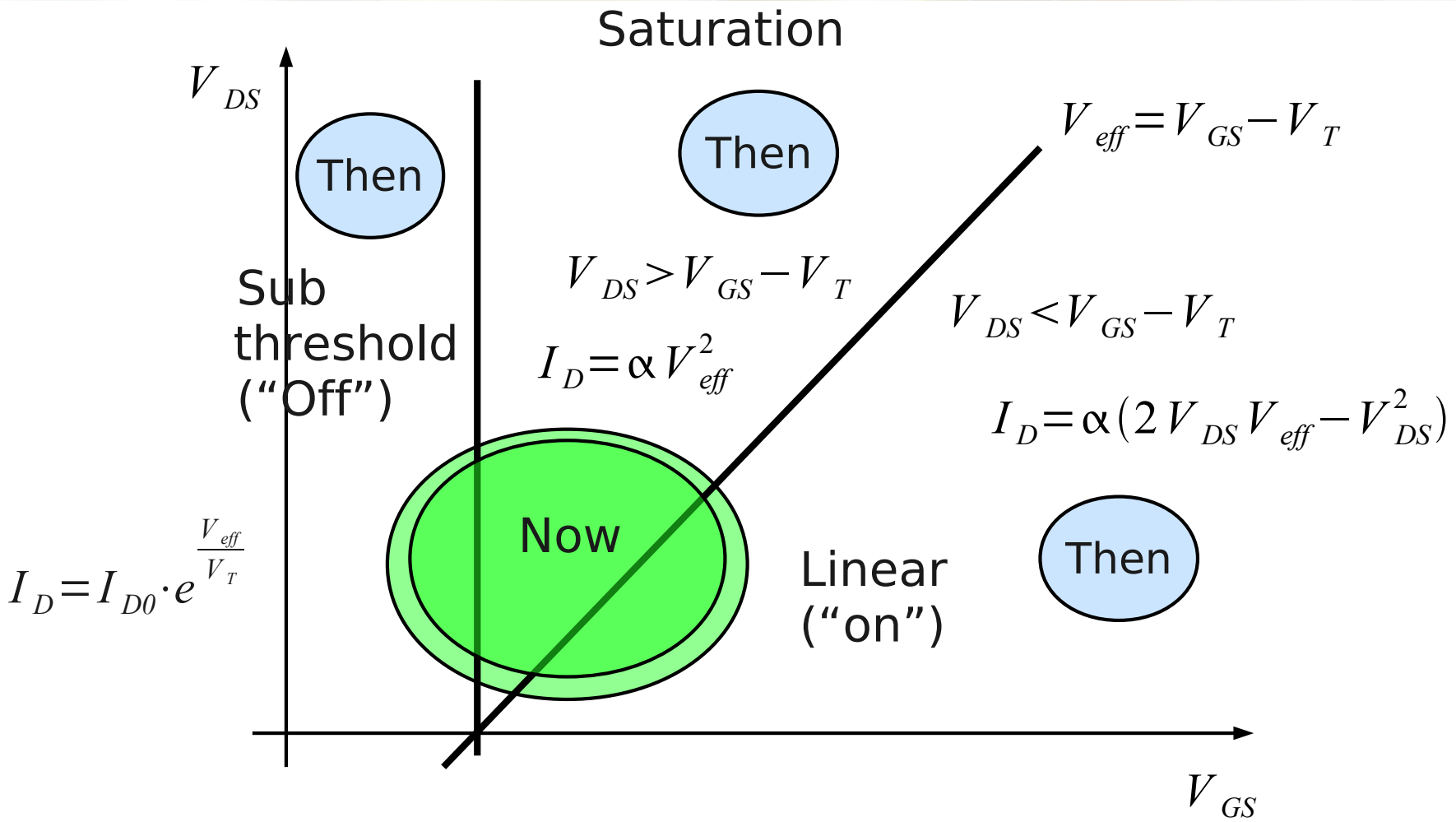
$$V_{eff} > 0,\ V_{ds} < V_{eff}$$

Saturation (high gain)

$$I \approx \alpha V_{eff}^2$$

$$V_{eff} > 0,\ V_{ds} > V_{eff}$$

Arbetsområden, forts



Andra ordningens effekter

Subthreshold **Linear** **Saturation**

$$I \approx I_{D0} \cdot e^{\frac{V_{eff}}{kT/q}}$$

$$I \approx \alpha \cdot \left(2 V_{eff} V_{ds} - V_{ds}^2 \right)$$

$$I \approx \alpha V_{eff}^2 \cdot \left(1 + \frac{V_{ds}}{V_\theta} \right)$$

$$V_T = V_{T0} + \gamma \cdot \left(\sqrt{2\Phi_F - V_{BS}} - \sqrt{2\Phi_F} \right), \; V_\theta = 1/\lambda$$

The första förstärkaren

En common-source förstärkare

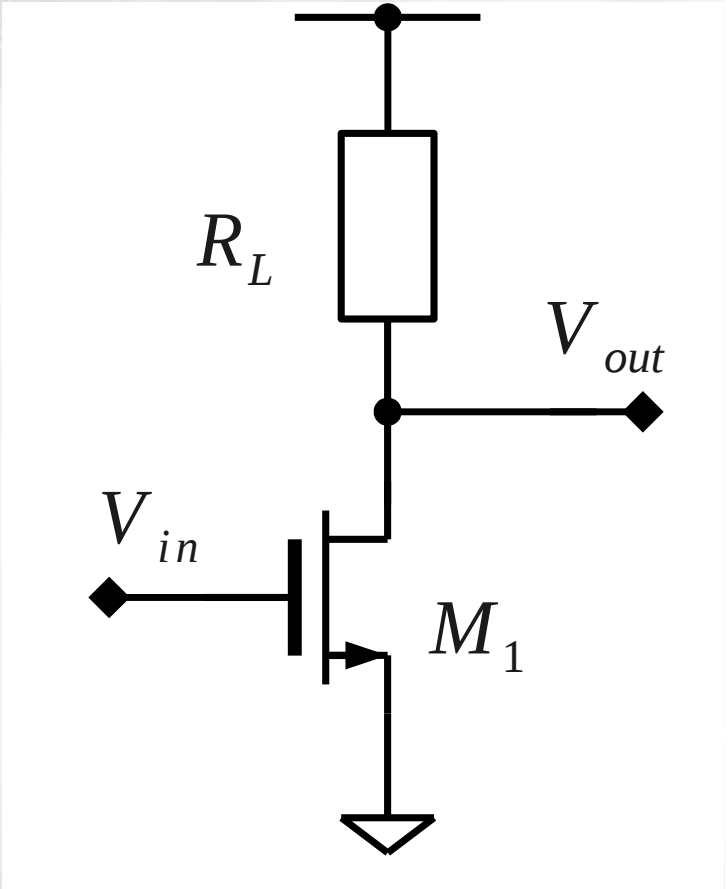
$$v_{out} = V_{DD} - R_L \cdot I_D$$

Mättade området

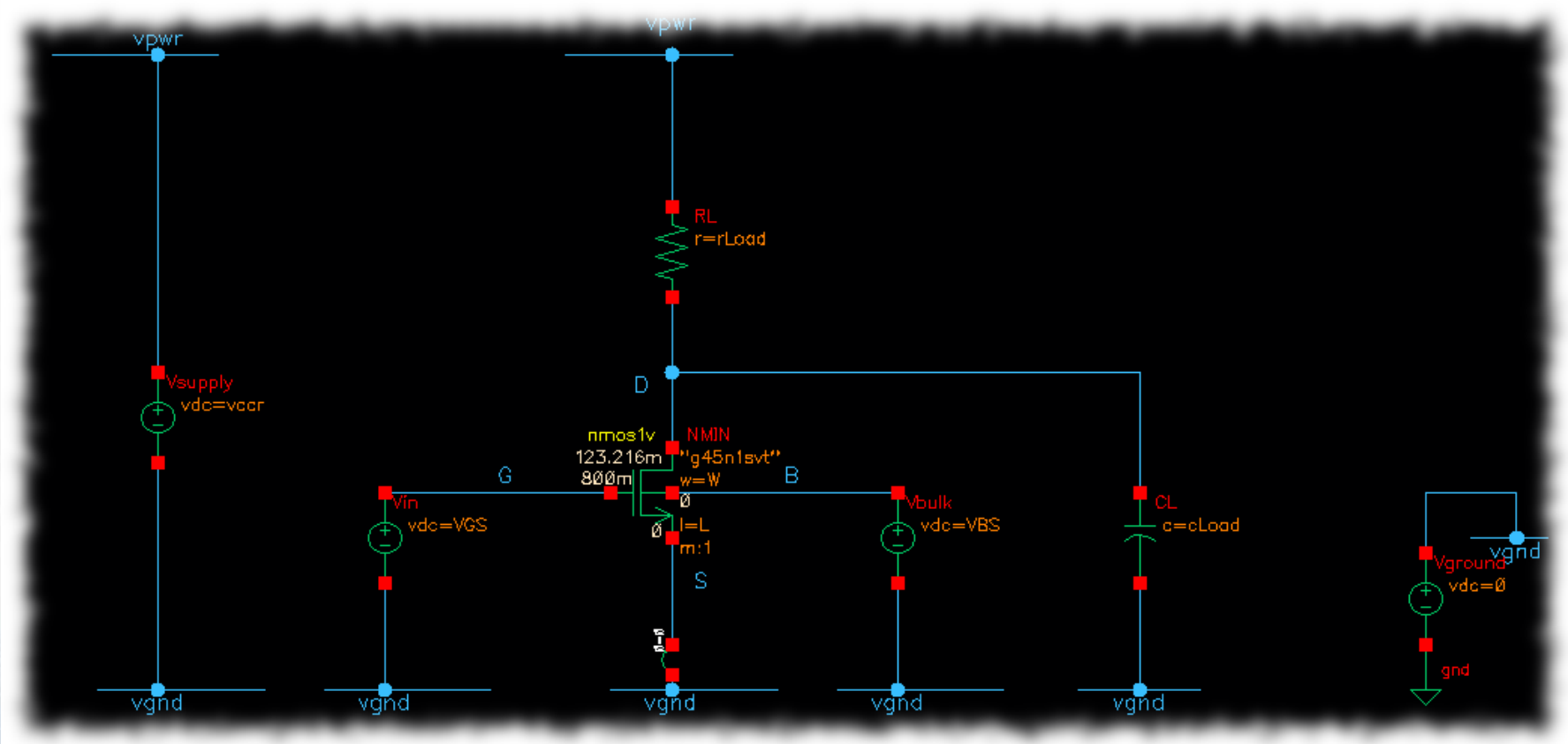
$$v_{out} = V_{DD} - R_L \cdot \alpha \cdot v_{eff}^2$$

Linjära området

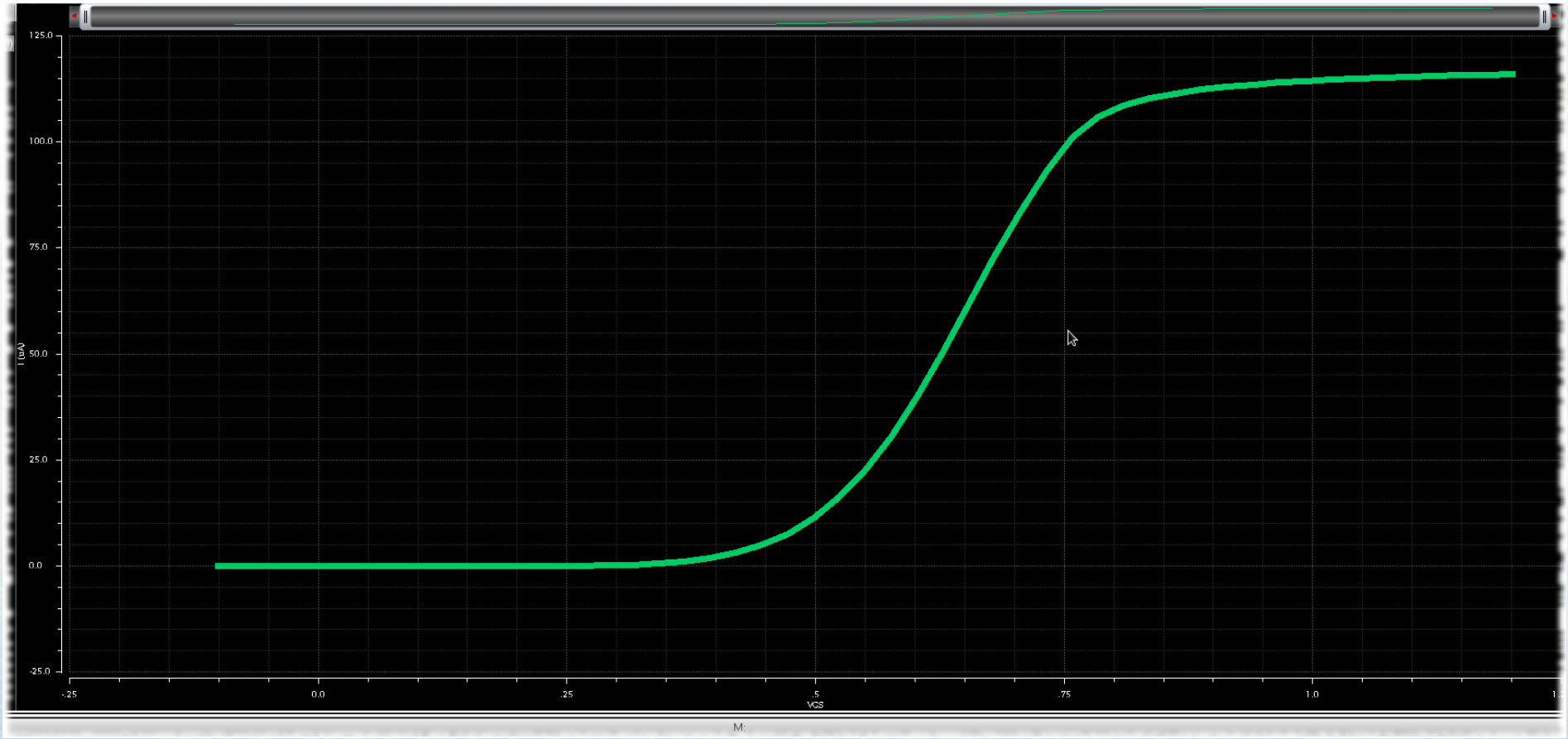
$$v_{out} = V_{DD} - R_L \cdot \alpha \cdot \left(2 v_{out} v_{eff} - v_{out}^2 \right)$$



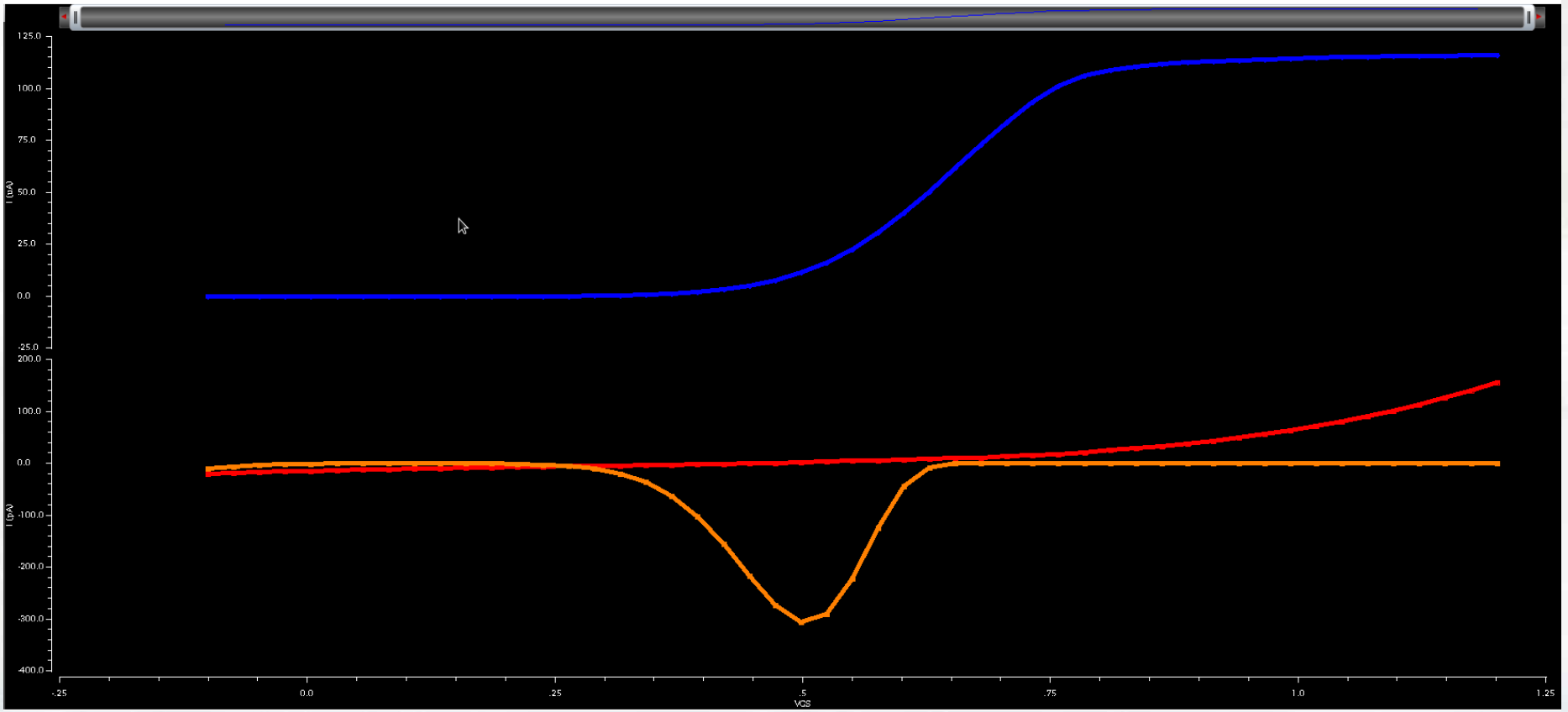
En enkel testbädd



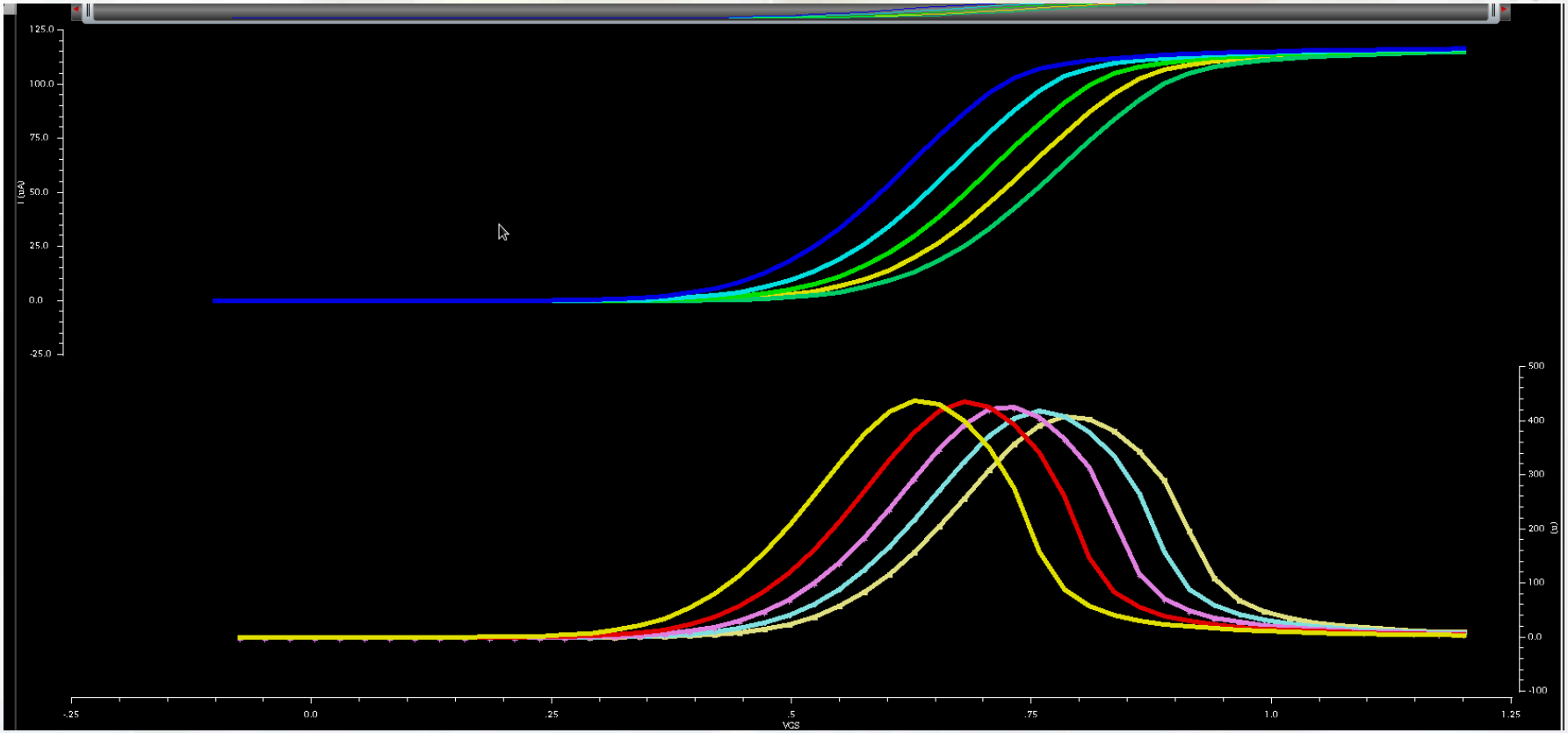
Simuleringsresultat, drainström



Andra ordningens effekter



Andra ordningens effekter, forts



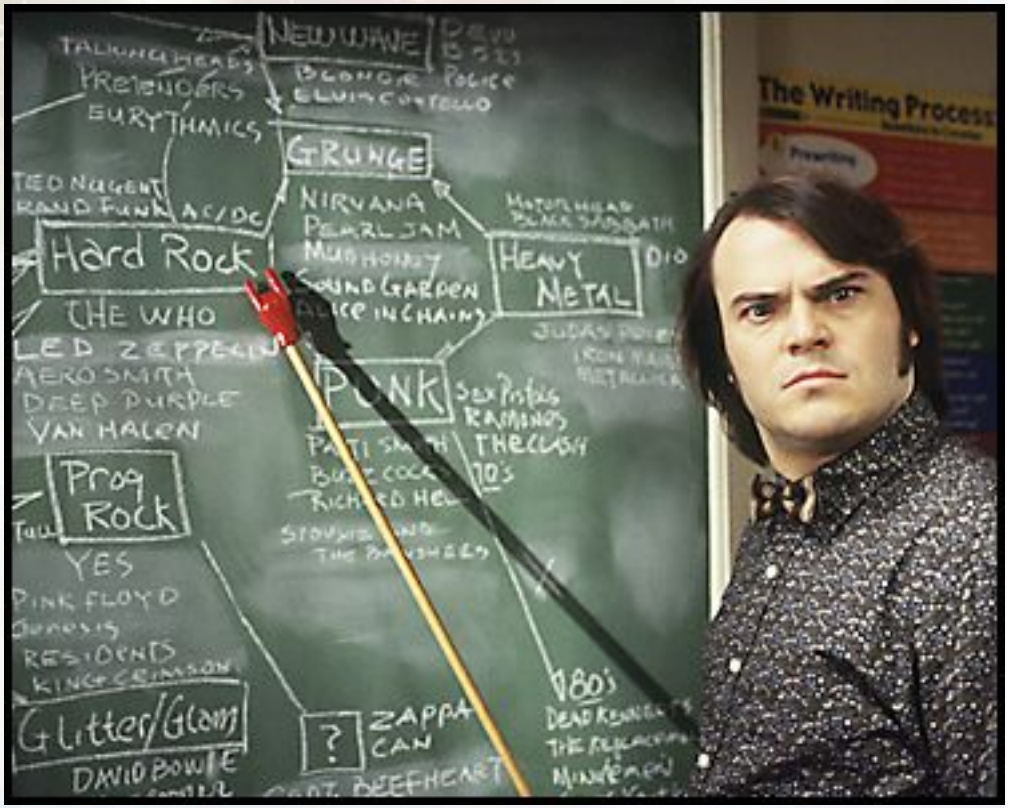
The derivative (lower graph) is the DC gain. The peak is reduced.

På tavlan ...

Storsignalschema

Småsignalschemat

Arbetspunkter



Vad gjorde vi idag?

Kursintroduktion

Labbar, quizzar, examination, osv

Transistor

Arbetsområden

En första förstärkare

Vad står på tur nästa gång?

Småsignalscheman

Fler analoga byggblock

Common-source, common-drain, common-gate, osv

Stabilitet

Föreläsning 2, Byggstenar

CMOS, Analog byggstenar

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Vad gjorde vi förra gången?

Introduktion

Labbar, quizzar, examination, osv

The CMOS transistor

PMOS vs NMOS

Arbetsområden (cut-off, linear, saturation)

Beteende

Första common-sourceförstärkaren

Vad kommer vi göra idag?

Småsignalscheman

Linearisering

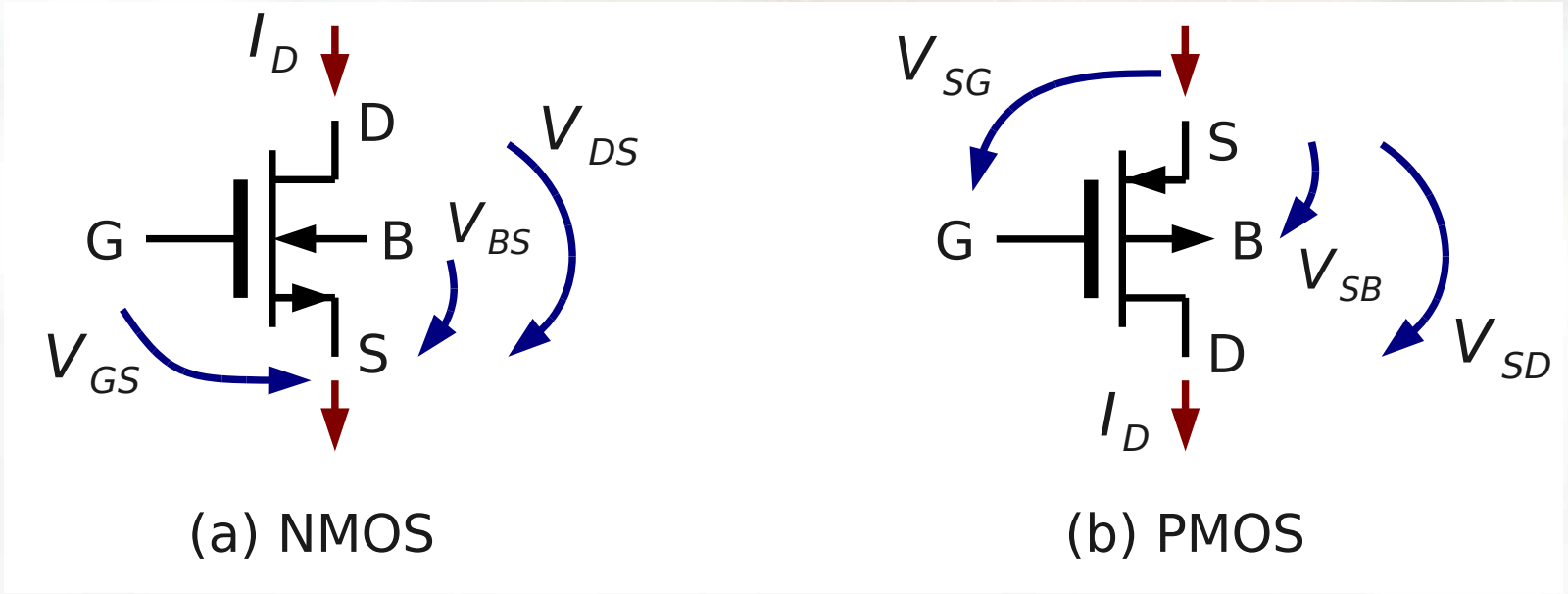
Analoga byggstenar

Common-source, common-drain, common-gate, etc.

Frekvensdomänen

Dominanta poler, multipla poler, stabilitet, med mera

Transistorn igen



Första förstärkaren igen

En common-sourceförstärkare

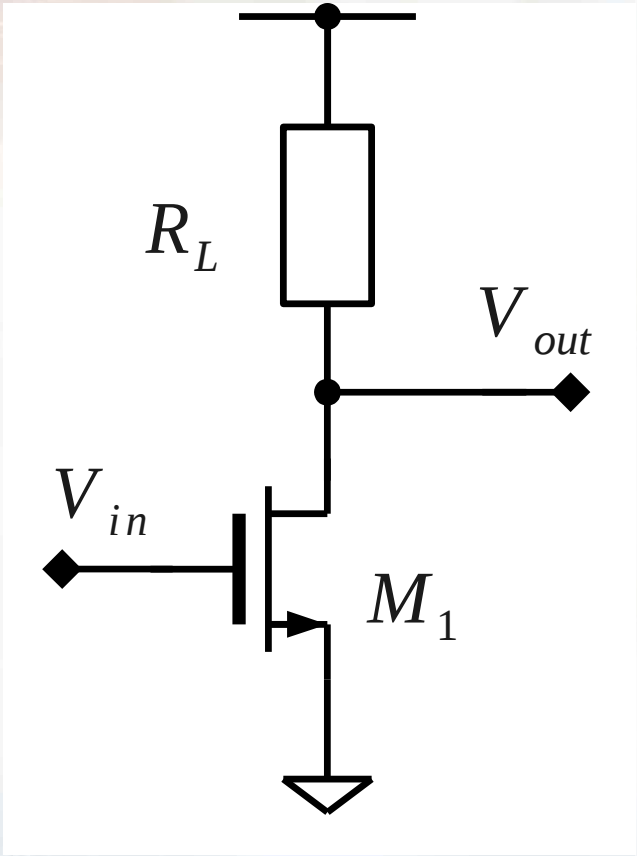
$$v_{out} = V_{DD} - R_L \cdot I_D$$

Mättade området (önskat, varför då?)

$$v_{out} = V_{DD} - R_L \cdot \alpha \cdot v_{eff}^2$$

Linjära området

$$v_{out} = V_{DD} - R_L \cdot \alpha \cdot \left(2 v_{out} v_{eff} - v_{out}^2\right)$$

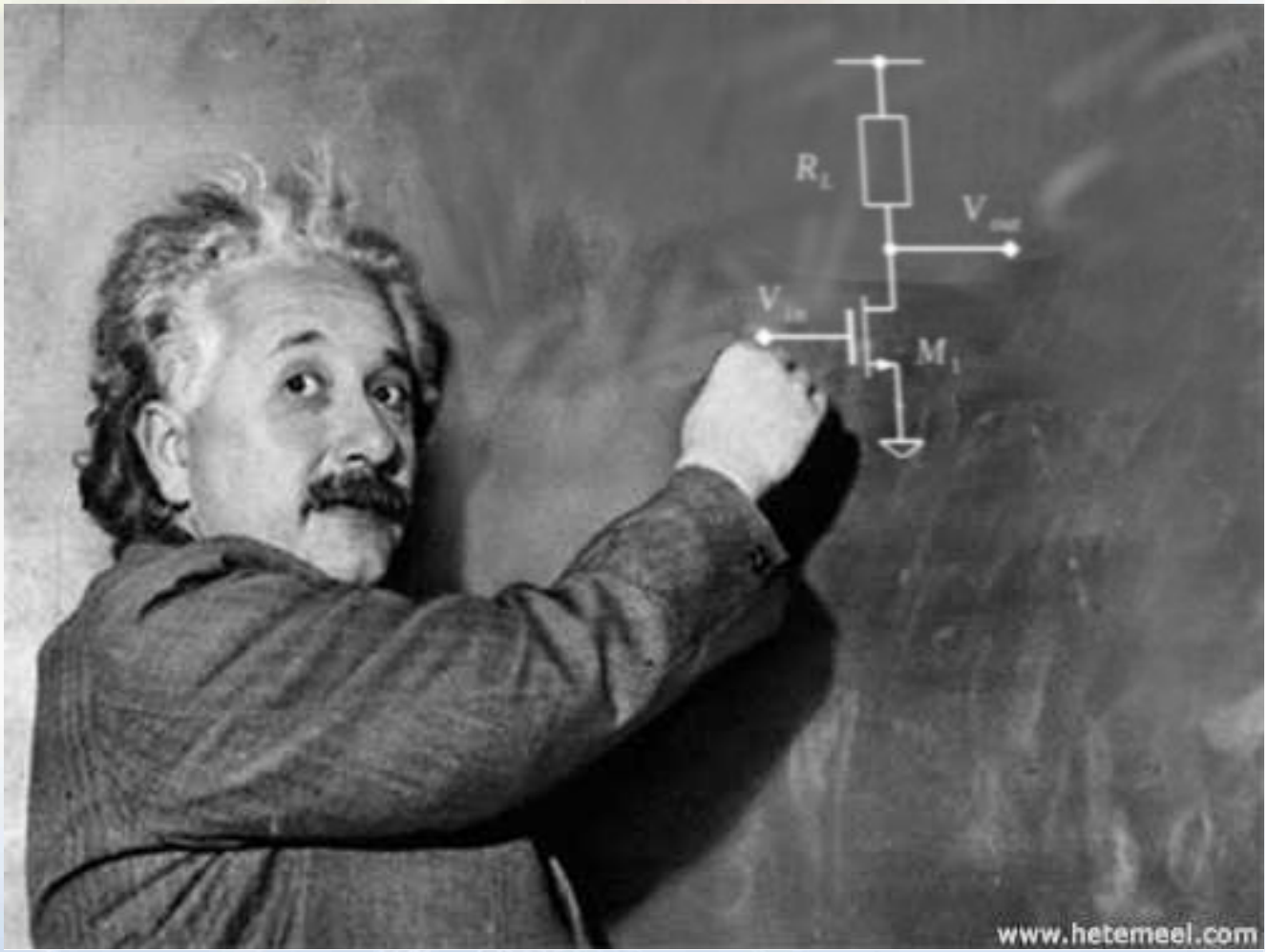


Första förstärkaren igen

Storsignal

Arbetspunkt

Andra krav



Småsignalschemat

Linearisering kring en arbetspunkt

Assume small variations around the DC point

Superimpose contributions from all sources to the output

Linearization implies no distortion, no clipping, etc.

Notice that there might be a trade-off between swing and max gain

The choice of DC point is non-trivial... maximum gain? maximum swing?

Linearization example

Original

$$I_D = \frac{\mu C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{gs} - V_T)^2 \cdot \left(1 + \frac{V_{ds}}{V_\theta}\right)$$

Partiell derivering, dvs linearisering

$$\Delta I_D = \frac{d I_D}{d \mu} \cdot \Delta \mu + \frac{d I_D}{d C_{ox}} \cdot \Delta C_{ox} + \frac{d I_D}{d W} \cdot \Delta W + \frac{d I_D}{d L} \cdot \Delta L +$$
$$+ \frac{d I_D}{d V_{GS}} \cdot \Delta V_{GS} + \frac{d I_D}{d V_T} \cdot \Delta V_T + \frac{d I_D}{d V_{DS}} \cdot \Delta V_{DS} + \frac{d I_D}{d V_\theta} \cdot \Delta V_\theta$$

Linearization example, cont'd

We assume the physical parameters to be constant

$$\Delta I_D = \frac{d I_D}{d V_{GS}} \cdot \Delta V_{GS} + \frac{d I_D}{d V_{DS}} \cdot \Delta V_{DS} + \frac{d I_D}{d V_T} \cdot \Delta V_T$$

Apply the chain rule

$$\frac{d I_D}{d V_T} \cdot \Delta V_T = \frac{d I_D}{d V_T} \cdot \frac{d V_T}{d V_{BS}} \cdot \Delta V_{BS}$$

Linearization example, cont'd

Introduce some nomenclature

$$\Delta I_D = \underbrace{\frac{dI_D}{dV_{GS}}}_{g_m} \cdot \Delta V_{GS} + \underbrace{\frac{dI_D}{dV_{DS}}}_{g_{ds}} \cdot \Delta V_{DS} + \underbrace{\frac{dI_D}{dV_T} \cdot \frac{dV_T}{dV_{BS}}}_{g_{mbs}} \cdot \Delta V_{BS}$$

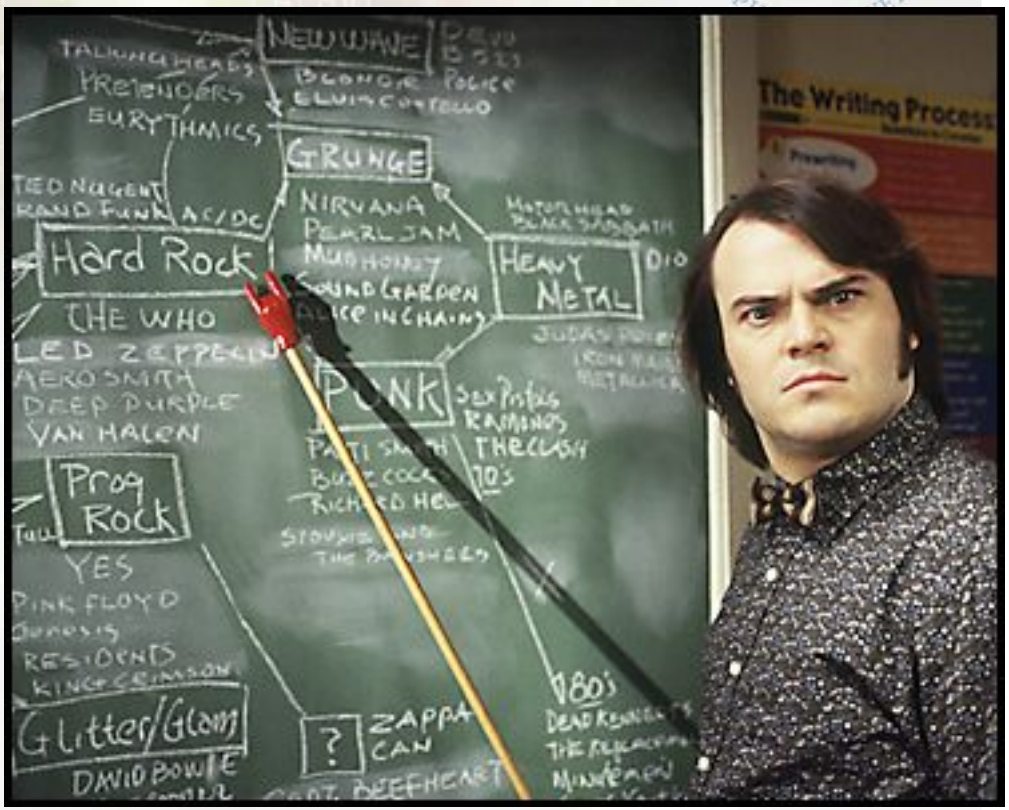
and skip the deltas

$$i_d = g_m \cdot v_{gs} + g_{ds} \cdot v_{ds} + g_{mbs} \cdot v_{bs}$$

En transistor som består av tre strömkällor

The small signal model and its impact

Illustrating the small signal model



Some calculations

(More practice in the lessons)

Transistors compiled

Parameter	Cut-off	Linear	Saturation
g_m	$\frac{\kappa I_D}{kT/q}$	$2\alpha v_{ds}$	$\frac{2I_D}{v_{eff}}$ and $2\sqrt{\alpha I_D}$
g_{mbs}	$g_m \cdot \frac{1-\kappa}{\kappa}$	$g_m \cdot \frac{\gamma}{2\sqrt{V_{SB}+2\varphi_F}}$	$g_m \cdot \frac{\gamma}{2\sqrt{V_{SB}+2\varphi_F}}$
g_{ds}	λI_D	$2\alpha\left(v_{eff}-v_{ds}\right)$	λI_D

Hur stora är dessa värden?

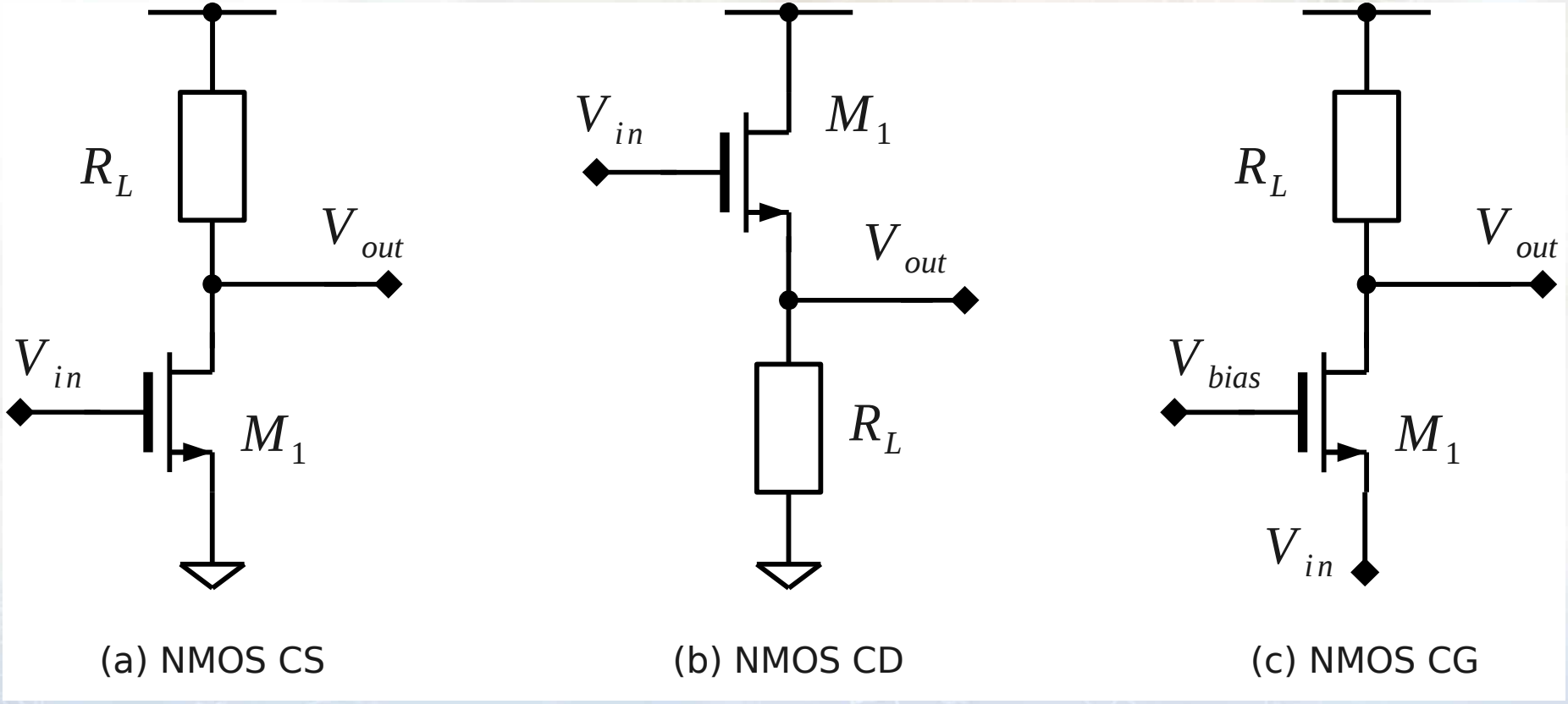
Transistor gain vs region

Expression	Cut-off	Linear	Saturation	
$A = \frac{g_m}{g_{ds}}$	$\frac{\kappa \cdot q}{\lambda \cdot k T}$	$\frac{v_{ds}}{v_{eff} - v_{ds}}$	$\frac{2}{\lambda \cdot v_{eff}}$	$\frac{2\sqrt{\alpha}}{\lambda \sqrt{I_D}}$

Where is highest gain?
$\kappa \approx 0.75$ and $kT/q \approx 26$ mV.

The three amplifier stages

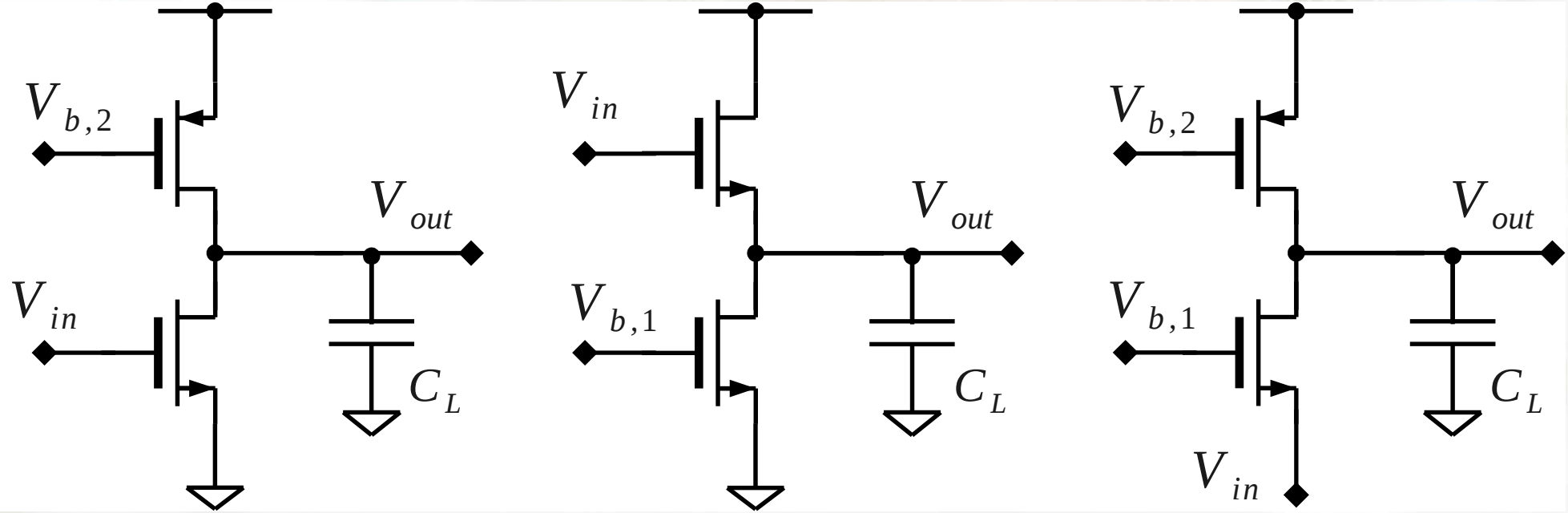
With passive load



(a) NMOS CS (b) NMOS CD (c) NMOS CG

The three amplifier stages, cont'd

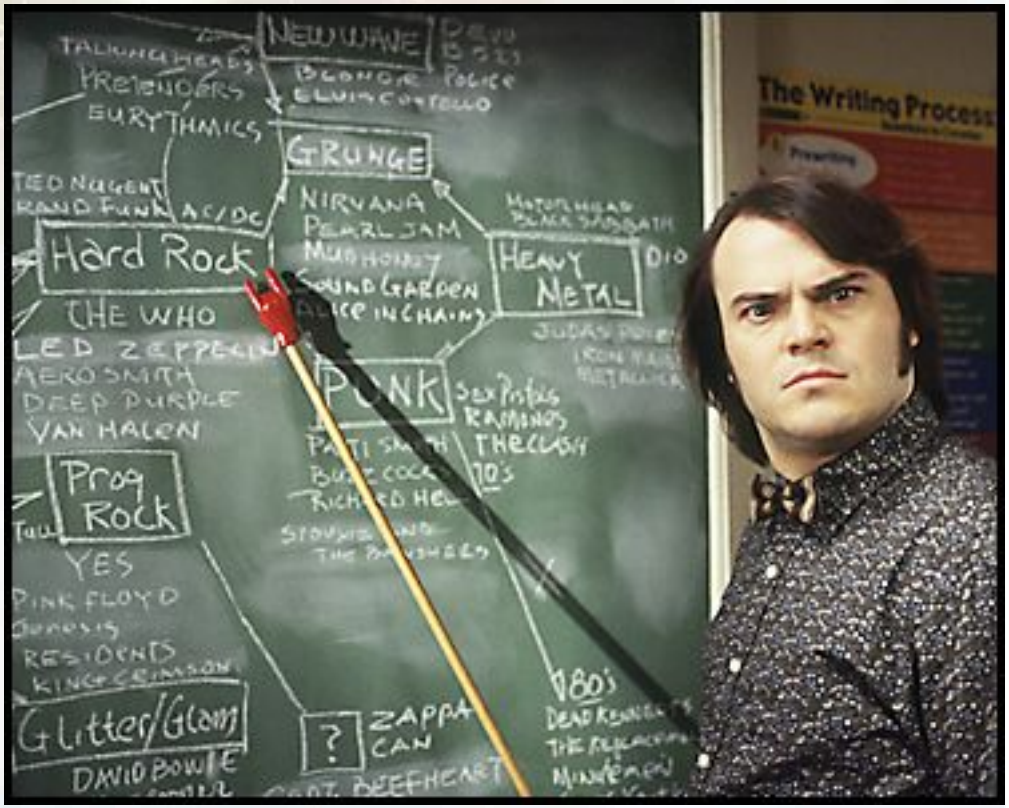
With active load



Why active load?

The small signal exercises

Using the small signal approach to derive the gain



Amplifier stages, compiled 1

Expression	CS	CD	CG
DC gain, $A_0 \approx g_m / g_{out}$	$\approx \frac{g_m}{g_P + g_N}$	$\approx \frac{g_m}{g_m + g_P + g_N} \approx 1$	$\approx \frac{g_m}{g_P + g_N}$
Output impedance, $\approx g_{out}$	$\approx g_P + g_N$	$\approx g_m$	$\approx g_P + g_N$
Input impedance, $\approx g_{in}$	∞	∞	$\approx g_m$
Bandwidth, $p_1 \approx g_{out} / C_L$	$\approx \frac{g_P + g_N}{C_L}$	$\approx g_m / C_L$	$\approx \frac{g_P + g_N}{C_L}$
Unity gain, $\approx A_0 \cdot p_1$	$\approx g_m / C_L$	N/A (why?)	$\approx g_m / C_L$

Amplifier stages, compiled 2

Expression	CS	CD	CG*)
DC gain, $A_0 \approx g_m / g_{out}$	$\approx 1/\lambda \cdot v_{eff}$	≈ 1	$\approx 1/\lambda \cdot v_{eff}$
Output impedance, $\approx g_{out}$	$\approx \lambda I_D$	$\approx 2 I_D / v_{eff}$	$\approx \lambda I_D$
Input impedance, $\approx g_{in}$	∞	∞	$\approx 2 I_D / v_{eff}$
Bandwidth, $p_1 \approx g_{out} / C_L$	$\approx \lambda I_D / C_L$	$\approx 2 I_D / C_L \cdot v_{eff}$	$\approx \lambda I_D / C_L \cdot v_{eff}$
Unity gain, $\approx A_0 \cdot p_1$	$\approx I_D / C_L \cdot v_{eff}$	N/A (why?)	$\approx I_D / C_L \cdot v_{eff}$

Amplifier stages, compiled 3

Amplifier	When and what to use?
Common-source	High-gain amplifier with high output impedance and high input impedance. Drives capacitive loads, typically in feedback configuration.
Common-gate	High-gain amplifier with high output impedance and "low" input impedance. Drives capacitive loads, typically in feedback configuration.
Common-drain	Low-gain amplifier with "low" output impedance and high input impedance. Drives resistive loads, can be in open-loop.

How to increase gain? Common-source stage

$$A = \frac{g_m}{g_{out}} = \frac{1}{\lambda \cdot v_{eff}} = \frac{2\sqrt{\alpha}}{\lambda\sqrt{I_D}}$$

Svaret beror på förspänningen

Minska v_{eff}

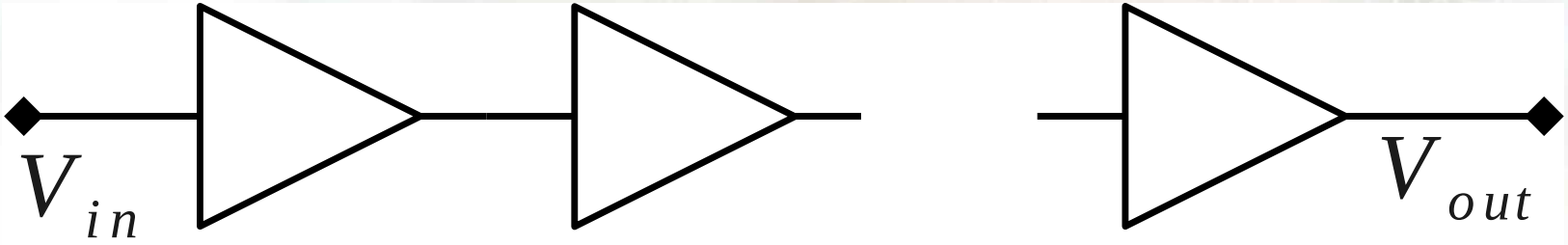
Minska $\lambda \sim 1/L$, i.e., increase the channel length.

Minska (!) strömmen I_D

Öka transistorstorlekarna, $\alpha \sim S \sim W$

Öka förstärkningen, det uppenbara sättet

Flera steg i serie där totala förstärkningen är produkten



Möjliggör högt sving

Drar en hel del effekt

Improving the gain, the electrical option

Revisit the expression on gain!

$$A = \frac{g_m}{g_{out}}$$

Increase the transconductance

Decrease output conductance (i.e., increase output impedance)

We've done that kind of, c.f., lowering the v_{eff}, etc.

Cascodes, the hardware option

Introduce more hardware to increase impedance

Cascodes increase the gain

How? - a small-signal exercise

We must balance the load

both in PMOS and NMOS "direction"

(Traditional way to maximize power efficiency)

So ... it's all about impedance levels

Cascodes

(Quickly) eats up the voltage headroom

For every diode-connected transistor, we loose one V_T of swing

We can save current since only one stage

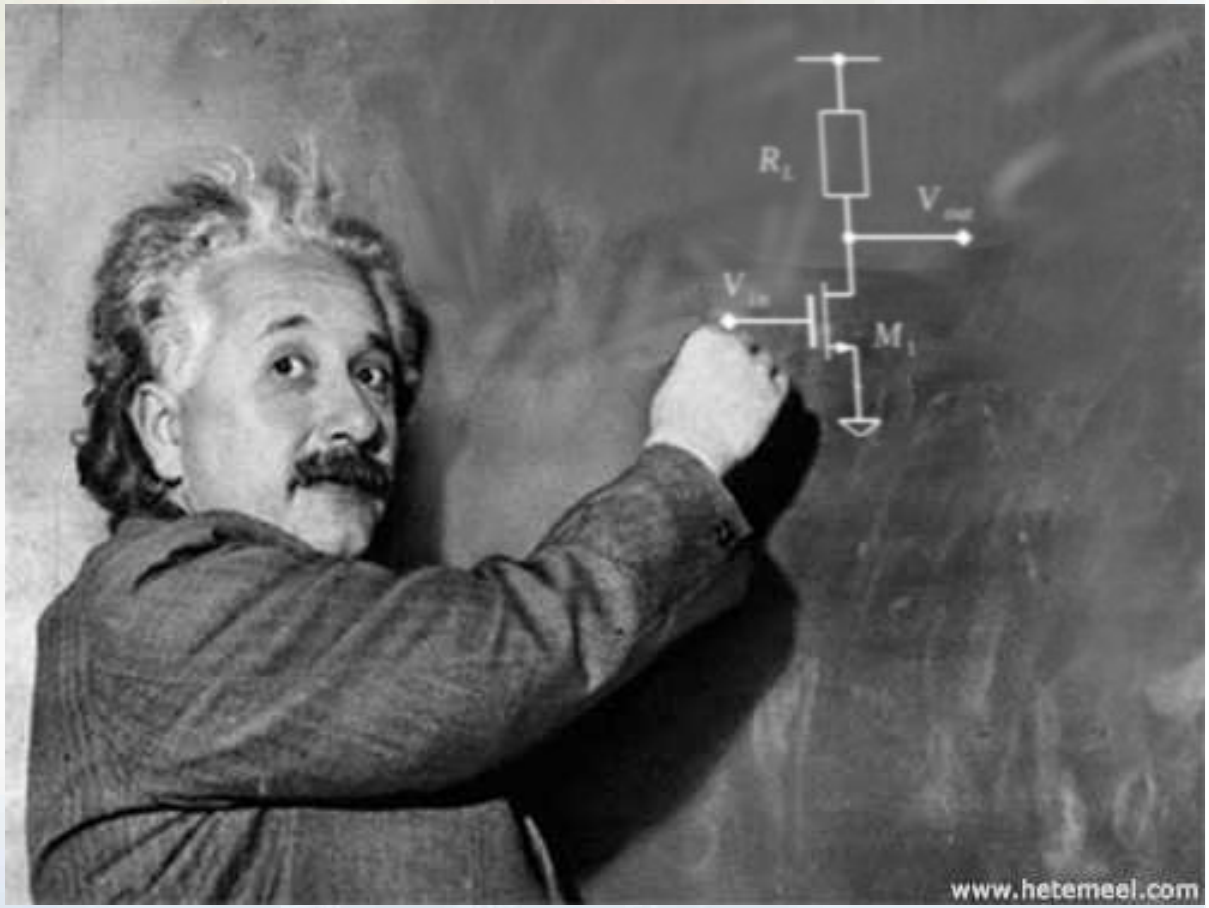
Complex biasing schemes

"The output impedance is multiplied"

Cascodes, common-source example

Voltage swing

Calculating the gain



Cascodes, common-source example

Formula still holds $A = g_m / g_{out}$ **and the output conductance is**

$$A = \frac{g_{m1}}{\frac{g_{n1} \cdot g_{n2}}{g_{m2}} + \frac{g_{p3} \cdot g_{p4}}{g_{m3}}} \approx \frac{g_{m1} \cdot g_{m2}}{2 \cdot g_{n1} \cdot g_{n2}}$$

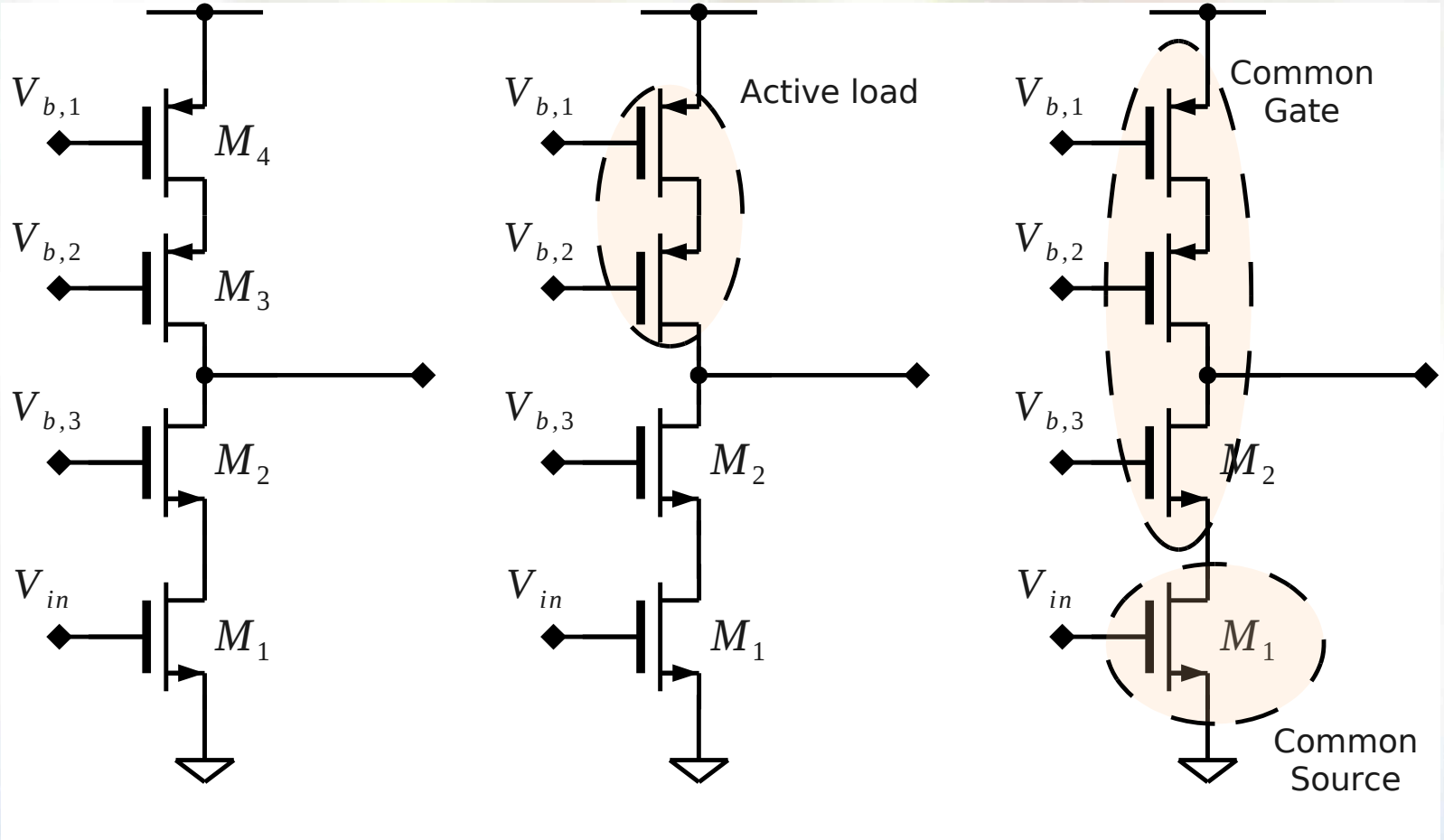
Now, we have some more handles to increase (set) the gain.

Effective voltage of input can be decoupled.

Classical analog trade-offs to distribute the gain).

But ... what happens to the gain if
the impedance levels are not balanced?

Cascodes are also multiple stages ...



Some conlusions on one slide

Cascodes eat up the swing

Cascodes save current compared to multi-stage

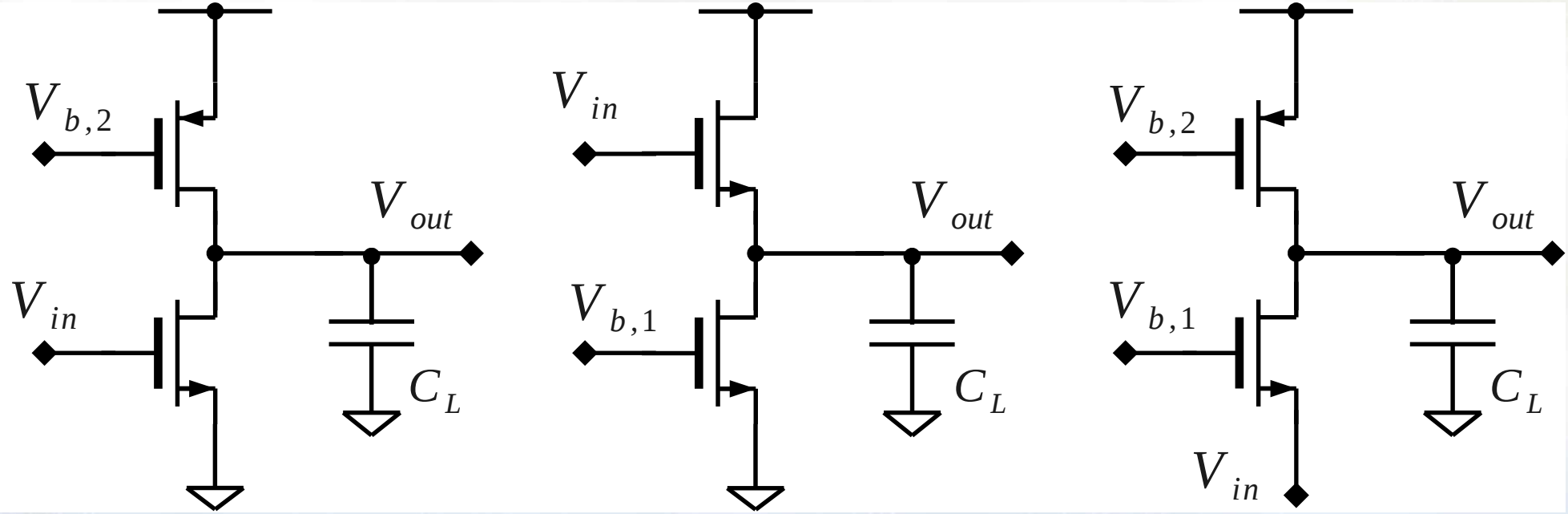
Cascodes and multi-stage have comparatively same area

Cascodes have more complex biasing schemes compared to multi-stage amplifiers

Cascodes might not be feasible in future designs!

The frequency domain

Include the capacitor in your calculations



The frequency domain

Small-signal exercise

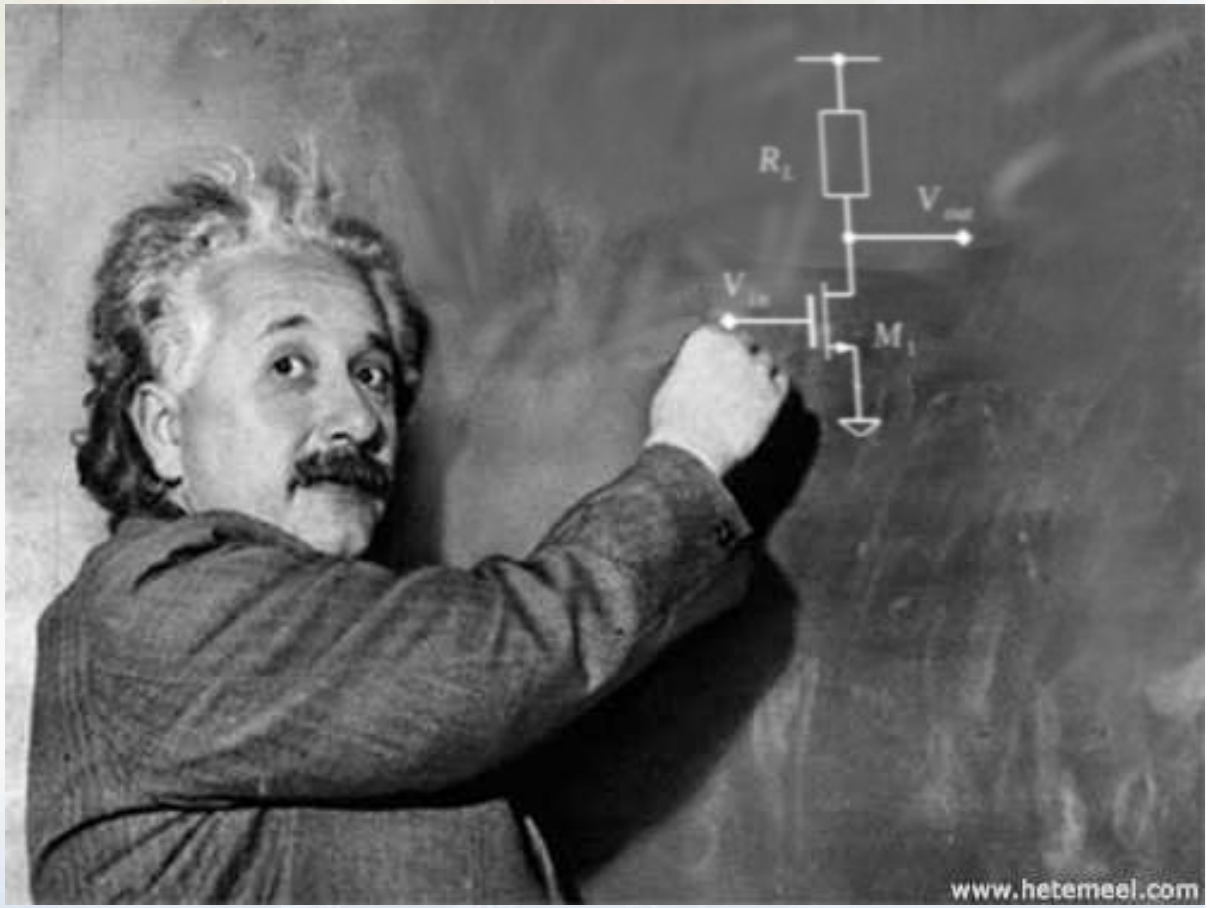
Impact of capacitor on common-source stage

Bode plot

Pole

DC gain

Unity-gain frequency



Sammanfattning

Bodes normalform

$$A(s) = \frac{A_0}{1 + \frac{s}{p_1}} = \frac{g_m / g_{out}}{1 + \frac{s}{g_{out} / C_L}}$$

Notice the trade-off between bandwidth and gain!

$$A_0 \cdot p_1 \approx \omega_{ug}$$

Amplifier stages, compiled 1

Expression	CS	CD	CG*)
DC gain, $A_0 \approx g_m / g_{out}$	$\approx \frac{g_m}{g_P + g_N}$	$\approx \frac{g_m}{g_m + g_P + g_N} \approx 1$	$\approx \frac{g_m}{g_P + g_N}$
Output impedance, $\approx g_{out}$	$\approx g_P + g_N$	$\approx g_m$	$\approx g_P + g_N$
Bandwidth, $p_1 \approx g_{out} / C_L$	$\approx \frac{g_P + g_N}{C_L}$	$\approx g_m / C_L$	$\approx \frac{g_P + g_N}{C_L}$
Unity gain, $\approx A_0 \cdot p_1$	$\approx g_m / C_L$	N/A (why?)	$\approx g_m / C_L$

Amplifier stages, compiled 2

Expression	CS	CD	CG*)
DC gain, $A_0 \approx g_m / g_{out}$	$\approx \frac{1}{\lambda \cdot v_{eff}}$	≈ 1	$\approx \frac{1}{\lambda \cdot v_{eff}}$
Output impedance, $\approx g_{out}$	$\approx \lambda I_D$	$\approx \frac{2 I_D}{v_{eff}}$	$\approx \lambda I_D$
Bandwidth, $p_1 \approx g_{out} / C_L$	$\approx \frac{\lambda I_D}{C_L}$	$\approx \frac{2 I_D}{C_L \cdot v_{eff}}$	$\approx \frac{\lambda I_D}{C_L \cdot v_{eff}}$
Unity gain, $\approx A_0 \cdot p_1$	$\approx \frac{I_D}{C_L \cdot v_{eff}}$	N/A (why?)	$\approx \frac{I_D}{C_L \cdot v_{eff}}$

Föreläsning 3, Analoga kretsar 2, Förstärkning

LiU EXPANDING REALITY

Vad gjorde vi förra gången?

Introduktion

Labbar, quizzar, examination, osv

CMOS-transistorn

PMOS, NMOS

Arbetsområden (cut-off, linear, saturation)

Allmänt beteende och småsignalschema

Första common-sourceförstärkaren

Vad kommer vi göra idag?

Sammanfatta det där med CMOS

- Småsignalschema, dvs linearisering
- Storsignalegenskaper, dvs arbetsområden

Analoga byggstenar

- Common-source, common-drain, common-gate, etc.
- Aktiv last

Frekvensdomänen

- Dominanta poler, multipla poler, stabilitet, med mera

Flerstegsförstärkare

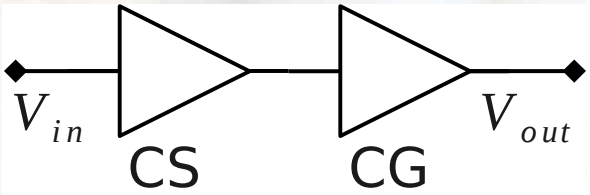
Single-stage (med kaskoder) vs two-stage?

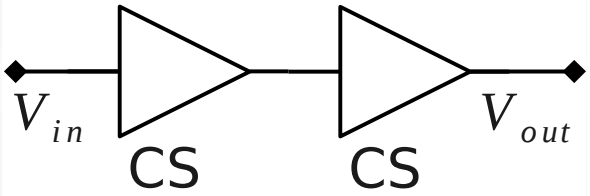
Samma DC förstärkning

Inte samma utimpedans

Flera poler (~ en per steg)

$$A(s)=\frac{A_1 \cdot A_2}{\left(1+\frac{s}{p_{11}}\right)\cdot\left(1+\frac{s}{p_{12}}\right)}$$





Flera poler införs

Fall 1 (CS+CG)

First amplifier sees low-impedance load: $(g_1+g_{m1})\|C_1 \approx g_{m1}\|C_1$

Second amplifier sees capacitive load: $g_{out} \approx g_2\|C_2$

Fall 2 (CS+CS)

First amplifier sees high-impedance load $(g_1+0)\|C_1 \approx g_1\|C_1$

Second amplifier sees capacitive load: $g_{out} \approx g_2\|C_2$

Notice that the g_2 in Case 2 is higher than g_2 in Case 1.

Oavsett vad du gör, finns återkoppling

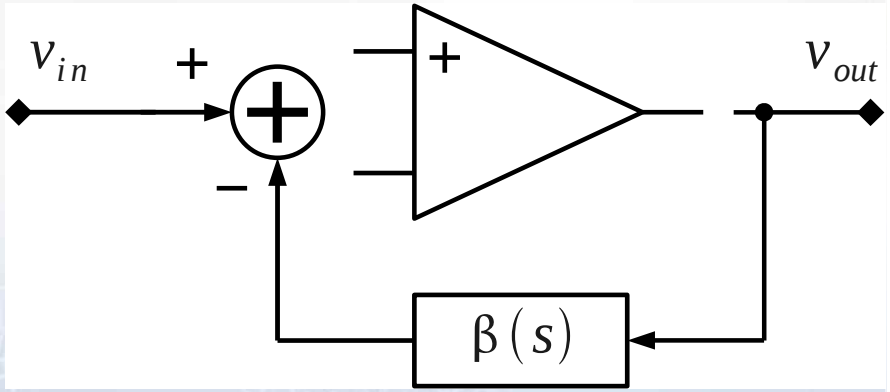
Vi har ett reglersystem

$$Y(s)=\left(X(s)-\beta(s)\cdot Y(s)\right)\cdot A(s)\Rightarrow$$

$$\frac{Y(s)}{X(s)}=\frac{A(s)}{1+\beta(s)\cdot A(s)}=\frac{1/\beta(s)}{1+\frac{1}{\beta(s)\cdot A(s)}}$$

En motkopplingsfaktor: $\beta(s)$

En slingförstärkning på: $\beta(s)\cdot A(s)$

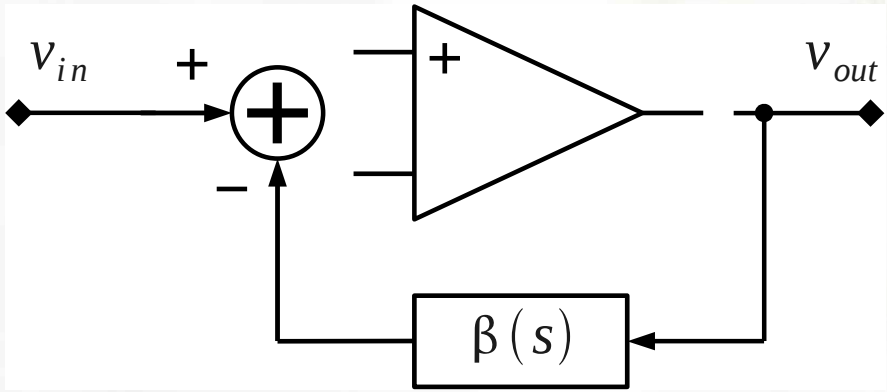


Varför vill man ha återkoppling?

Gain is now under control!

No variation with g_m/g_{ds}, instead given by (normally)

high-accuracy components



"Unlimited" drive capability

Isolation of input and output

Linearization

Remember, it is a regulation loop. It is designed to track the changes, anything added in the loop will be supressed.

Stability

Slarvigt sagt måste man undvika att följande inträffar

$$\beta(s)\cdot A(s)\neq -1$$

Då får vi en oändlig förstärkning i systemet

(In reality, the whole proof is quite complex.)

Fasmarginalen bestämmer hur långt vi är från detta

Dålig fasmarginal ger svängningar

Kritiskt dämpat vid ~ 70 grader (poler i det återkopplade systemet blir reella snarare än komplexpar).

Vad gjorde vi idag?

The most common amplifier stages

Frequency domain

Stability

Some top-level tips-and-tricks

Vad står på tur nästa gång?

More on amplifiers

Operational amplifiers

Differential amplifiers

Föreläsning 4, Stabilitet, Kompensering

Operational amplifiers, high-gain, high-speed

LiU EXPANDING REALITY

Vad gjorde vi förra gången?

Multi-stage amplifiers

- Increases gain
- Increases number of poles

Frequency domain

- Stability
- Phase margin

Vad kommer vi göra idag?

Wrap-up the discussion on compensation and stability

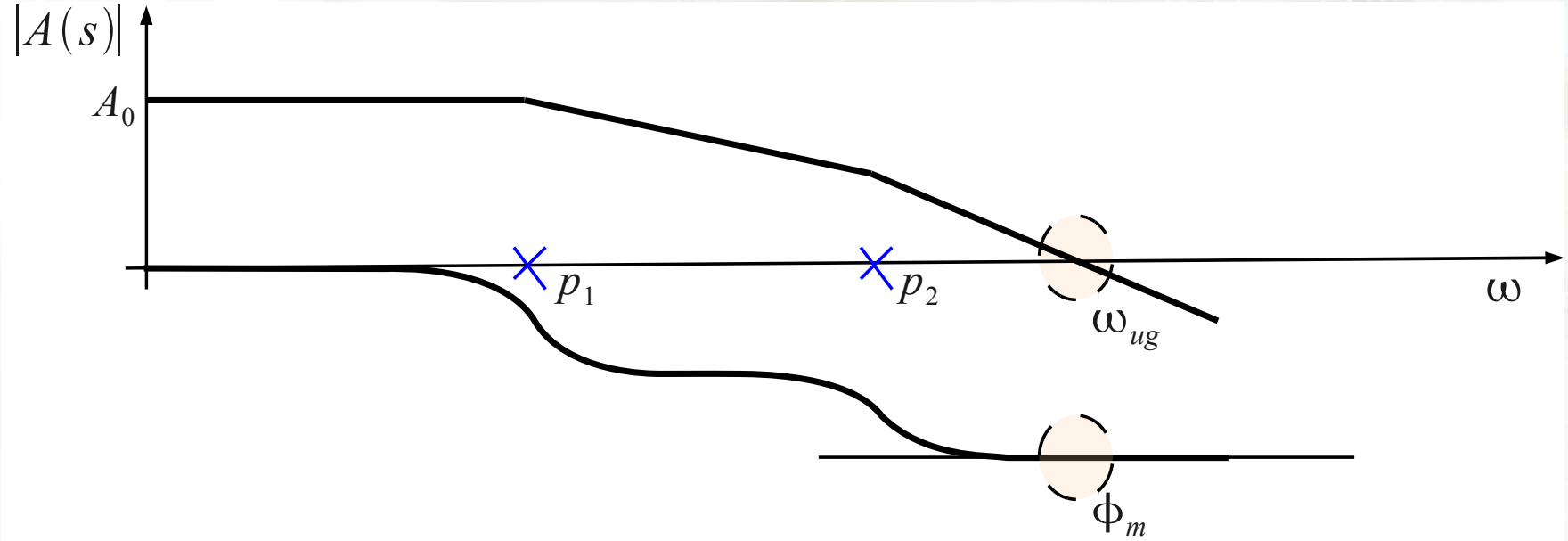
- Two-stage amplifiers
- Three compensation methods

Operational amplifiers

- Characteristics
- Typical operation and impact of limited accuracy

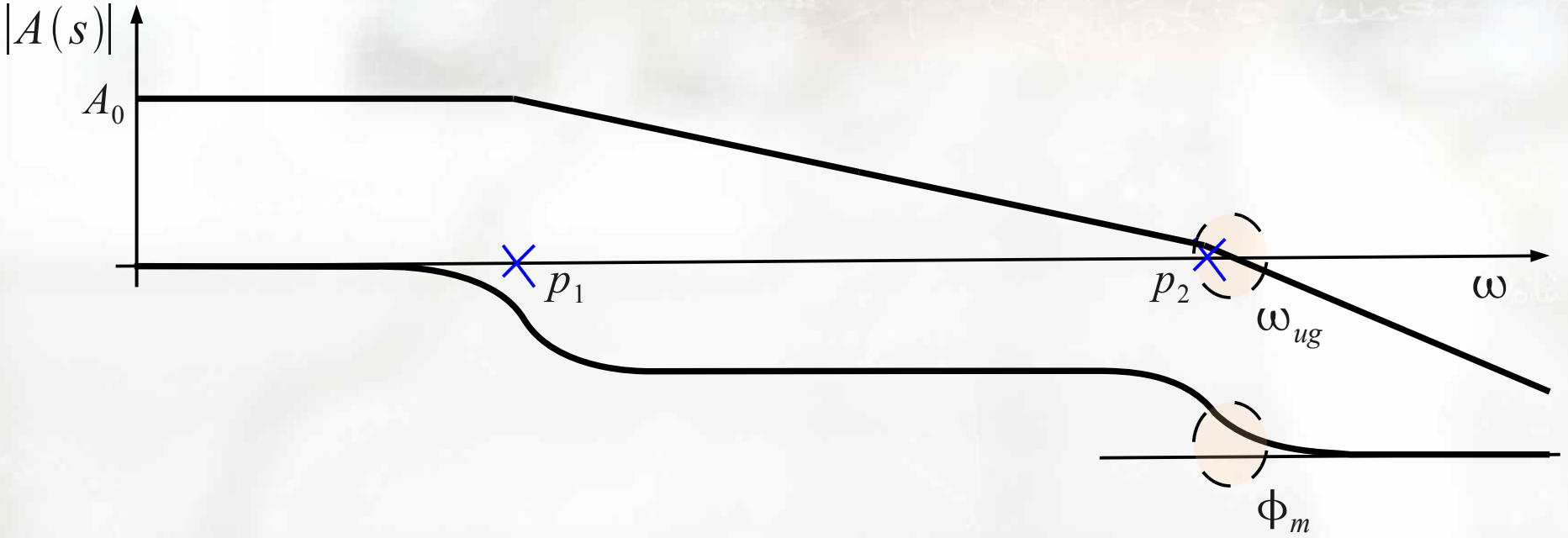
Poler och nollställen 1

Stable?



Poler och nollställen 2

Stable?

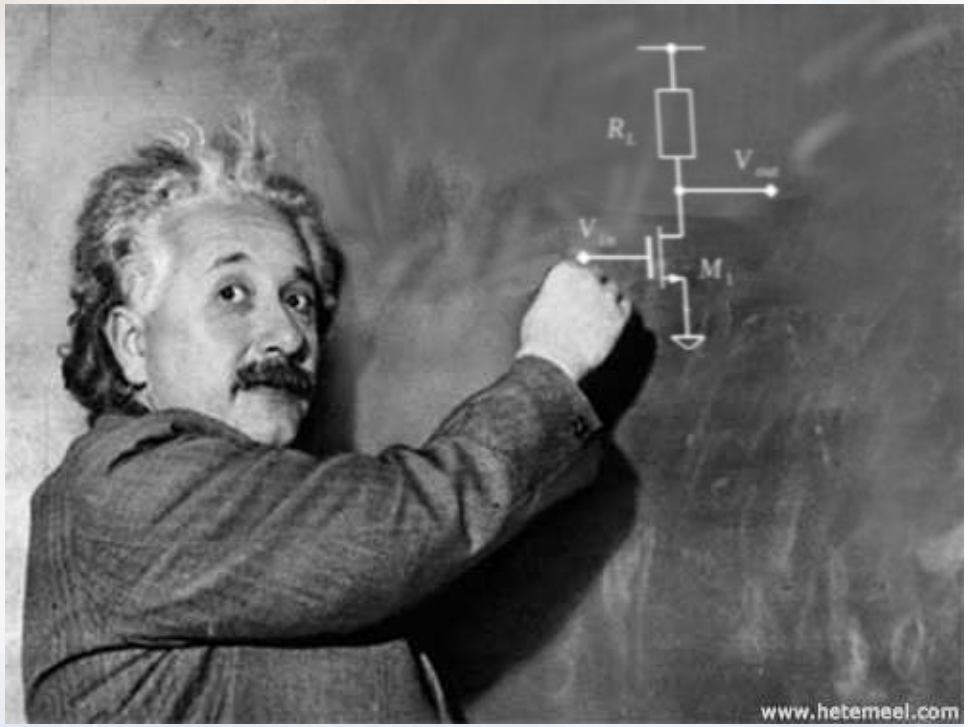


Stabilitet

Bode plot

Överföringsfunktion

Fasmarginal vs återkopplingsfaktor



Stegsvar

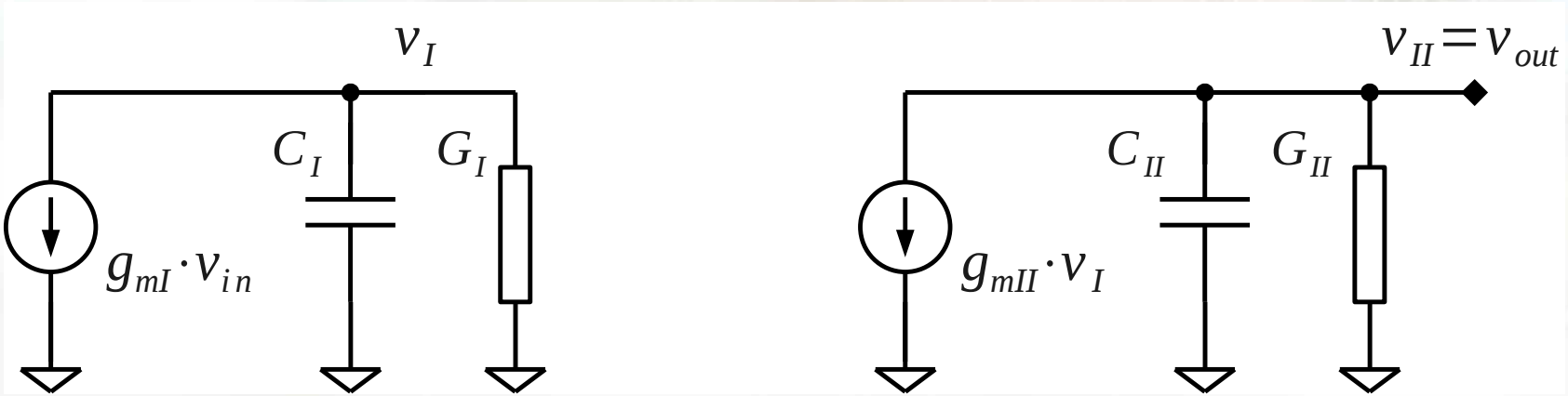
Settling

Oscillations

Critically damped at 70 degrees

Systematisk ansats

En modell (high-impedance load) - tvåpolssystem



$$p_1 = \frac{G_I}{C_I},\ p_2 = \frac{G_{II}}{C_{II}},\ A_1 = \frac{g_{mI}}{G_I},\ A_2 = \frac{g_{mII}}{G_{II}}$$

Dominant pole assumption (output)

Assuming pole splitting, $p_2 \gg p_1$, gives us

$$A(s) = \frac{A_1 \cdot A_2}{\left(1 + \frac{s}{p_{11}}\right) \cdot \left(1 + \frac{s}{p_{12}}\right)} \approx \frac{A_1 \cdot A_2}{1 + \frac{s}{p_1} + \frac{s^2}{p_1 \cdot p_2}}$$

This implies: $\omega_{ug} \approx A_1 \cdot A_2 \cdot p_1$ and

$$\phi_m = 180 - arg\, A(j\,\omega_{ug}) = 180 - atan\frac{\omega_{ug}}{p_1} - atan\frac{\omega_{ug}}{p_2} \approx 90 - atan\frac{\omega_{ug}}{p_2}$$

$$\phi_m \approx 90 - atan\left(A_0 \cdot \frac{p_1}{p_2}\right)$$

The formulas (dominant load!)

Unity-gain frequency

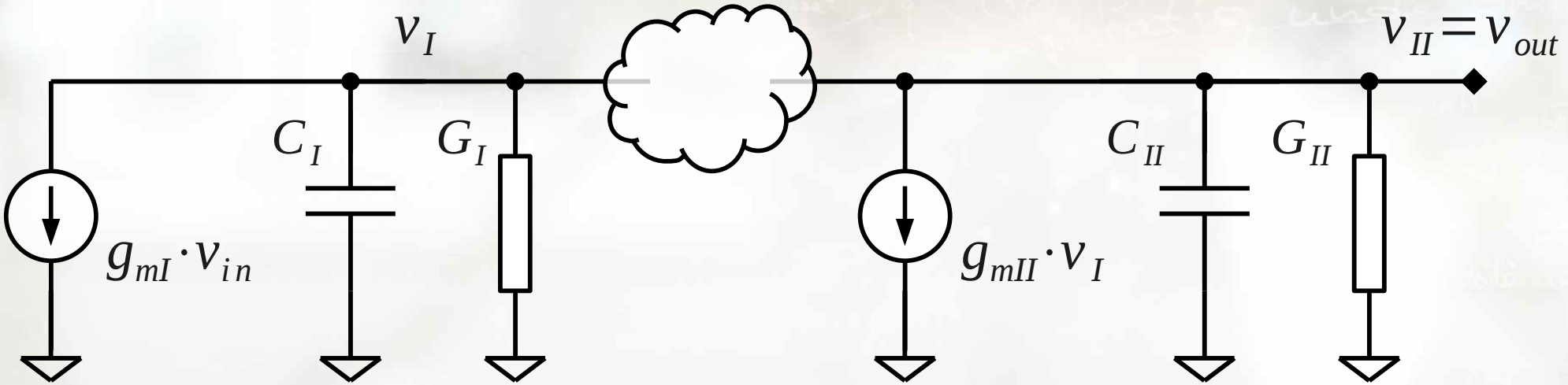
$$\omega_{ug} \approx \frac{g_{mI} \cdot g_{mII}}{G_I \cdot G_{II}} \cdot \frac{G_{II}}{C_{II}} = \frac{g_{mI} \cdot g_{mII}}{G_I \cdot C_{II}}$$

Phase margin

$$\varphi_m \approx 90 - atan\frac{\omega_{ug}}{p_2} = 90 - atan\frac{\frac{g_{mI} \cdot g_{mII}}{G_I \cdot C_{II}}}{\frac{G_I}{C_I}} = 90 - atan\frac{g_{mI} \cdot g_{mII} \cdot C_I}{G_I^2 \cdot C_{II}}$$

etc., etc., etc. -- We need to be a bit more organized...

Compensation, poles are too close



The "cloud" could be a capacitor or series resistor-capacitor.

Compensation, two cases:

1) "Internal" node sees a low-impedance node

Typically: output load dominates, drive a capacitive load
Load-compensation, i.e., increase cap externally

2) "Internal" node sees a high-impedance node

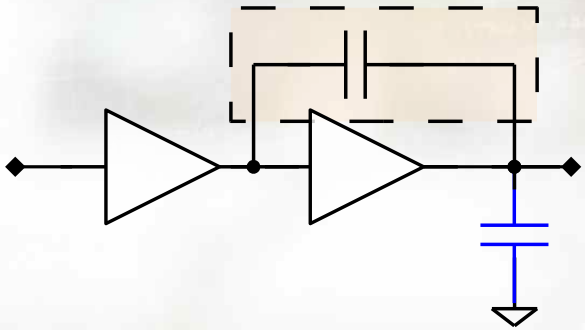
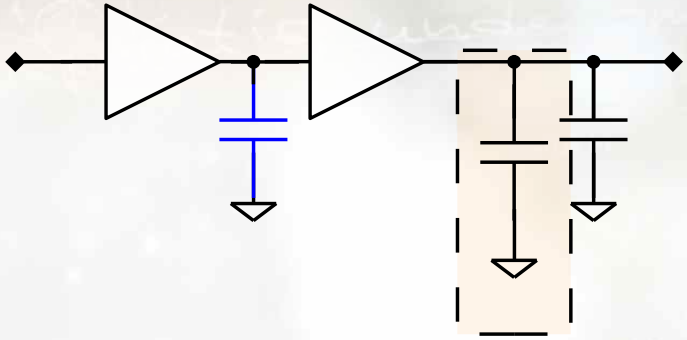
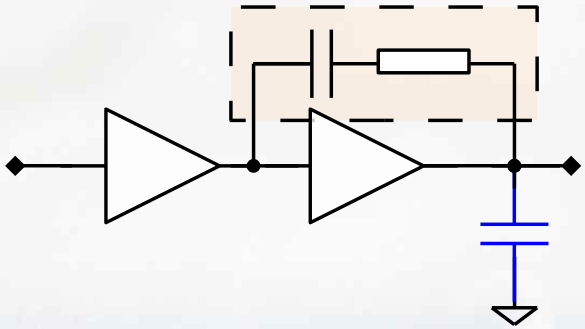
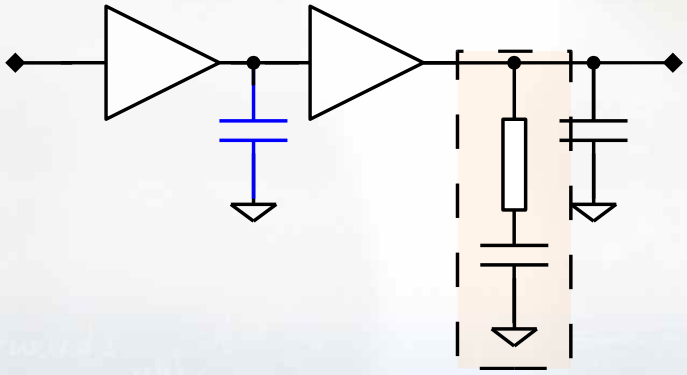
Typically: internal load dominates, drive a resistive load
Miller-compensation, i.e., utilize second-stage gain to multiply

C_C

As always, some exceptions to the rule:

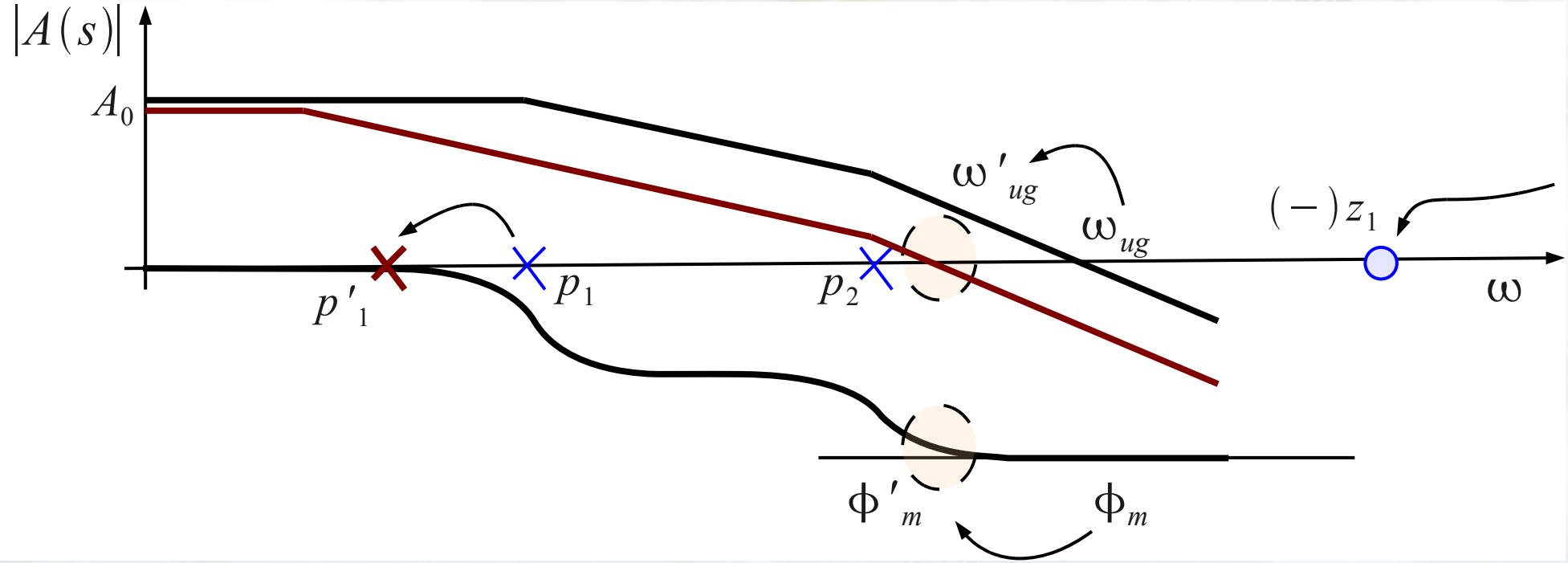
Nested compensation, active compensation, ... and more ...

Compensation compiled:

	Miller	Load compensation
Cap		
Cap + Res		

Compensation

What is the cost associated with compensation?



Compensation, Miller capacitance

Introduced zero	Parasitic pole	Dominant pole	Unity-gain
$z_1 = \frac{g_{mII}}{C_C}$	$p_2 = \frac{-g_{mII}}{C_{II}}$	$p_1 = \frac{-G_I \cdot G_{II}}{g_{mII} \cdot C_C}$	$\omega_{ug} = \frac{g_{mI}}{C_C}$

Introduced zero	Parasitic pole	Phase margin
$z_1 \approx 10 \cdot \omega_{ug}$	$p_2 \approx 2.2 \cdot \omega_{ug}$	≈ 60

Dominant pole moves "down", parasitic pole moves "up"

Parasitic zero added (harmful for phase margin)

Compensation, Nulling resistor 1

Introduced zero	Parasitic poles	Dominant pole	Unity-gain
$z_1 = \frac{g_{mII}}{C_C} \cdot \frac{1}{1 - R_Z \cdot g_{mII}}$	$p_2 = \frac{-g_{mII}}{C_{II}}$, $p_3 = \frac{-1}{R_Z \cdot C_{II}}$	$p_1 = \frac{-G_I \cdot G_{II}}{g_{mII} \cdot C_C}$	$\omega_{ug} = \frac{g_{mI}}{C_C}$

$$R_Z = \frac{1}{g_{mII}} \cdot \left(1 + \frac{C_{II}}{C_C}\right)$$

Introduced zero	Parasitic pole	Phase margin
$z_1 \rightarrow p_2$	$p_3 \approx 1.73 \cdot \omega_{ug}$	≈ 60

Compensation, Nulling resistor 2

Introduced zero	Parasitic poles	Dominant pole	Unity-gain
$z_1 = \frac{g_{mII}}{C_C} \cdot \frac{1}{1 - R_Z \cdot g_{mII}}$	$p_2 = \frac{-g_{mII}}{C_{II}}$, $p_3 = \frac{-1}{R_Z \cdot C_{II}}$	$p_1 = \frac{-G_I \cdot G_{II}}{g_{mII} \cdot C_C}$	$\omega_{ug} = \frac{g_{mI}}{C_C}$

$$R_Z = \frac{1}{g_{mII}}$$

Introduced zero	Parasitic pole	Phase margin
$z_1 \to \infty$	$p_2 \approx 1.73 \cdot \omega_{ug}$, $p_3 > 10 \cdot \omega_{ug}$	≈ 60

Rule-of-thumbs for hand-calculation

Use e.g. MATLAB to support calculations for understanding

```
/site/edu/es/ANTIK/antikLab/m/antikPoleZero.m
```

```
/site/edu/es/ANTIK/antikLab/m/antikSettling.m
```

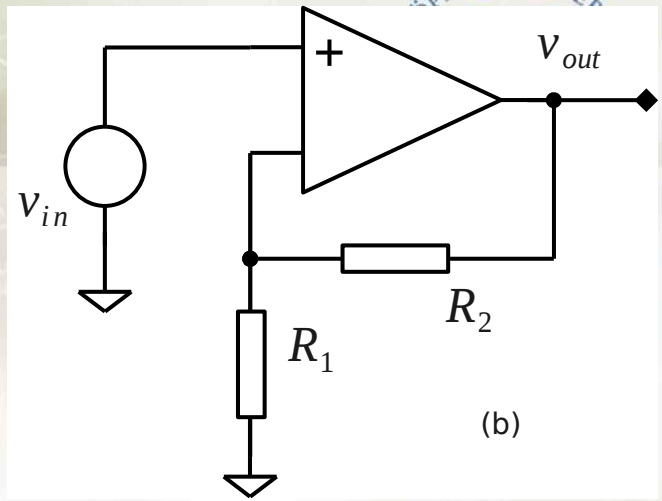
In the end, use the simulator.

Must be robust over temperature and other variations.
Hand calculations are incorrect per definition

Model corresponds quite well with circuit once you have identified the different stages

See for example exercises

Operational amplifiers



Drive resistive loads

have zero output impedance, zero input impedance, infinite gain

act like a voltage source

Operational transconductance amplifiers (OTA)

drive capacitive loads

infinite output impedance, zero input impedance, infinite gain

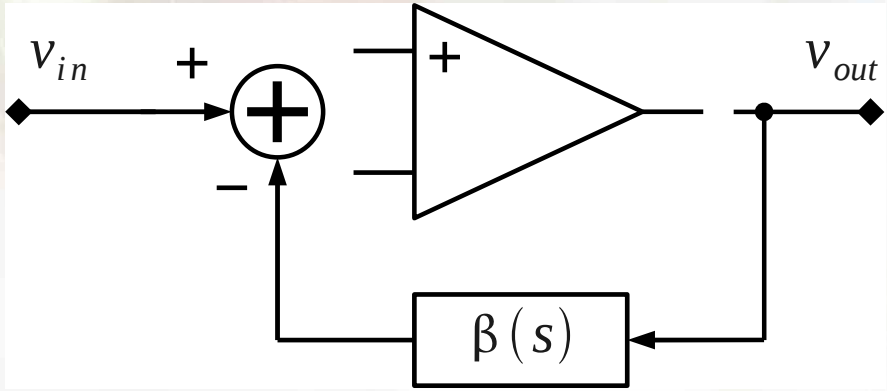
act like a current source

Why do you want controlled feedback?

Gain is now under control!

No variation with g_m / g_{ds}

instead it is given by passive components



"Unlimited" drive capability

Isolation of input and output

Linearization

Remember, it is a regulation loop. It is designed to track the changes, anything added in the loop will be supressed.

Practical concerns

Limited gain

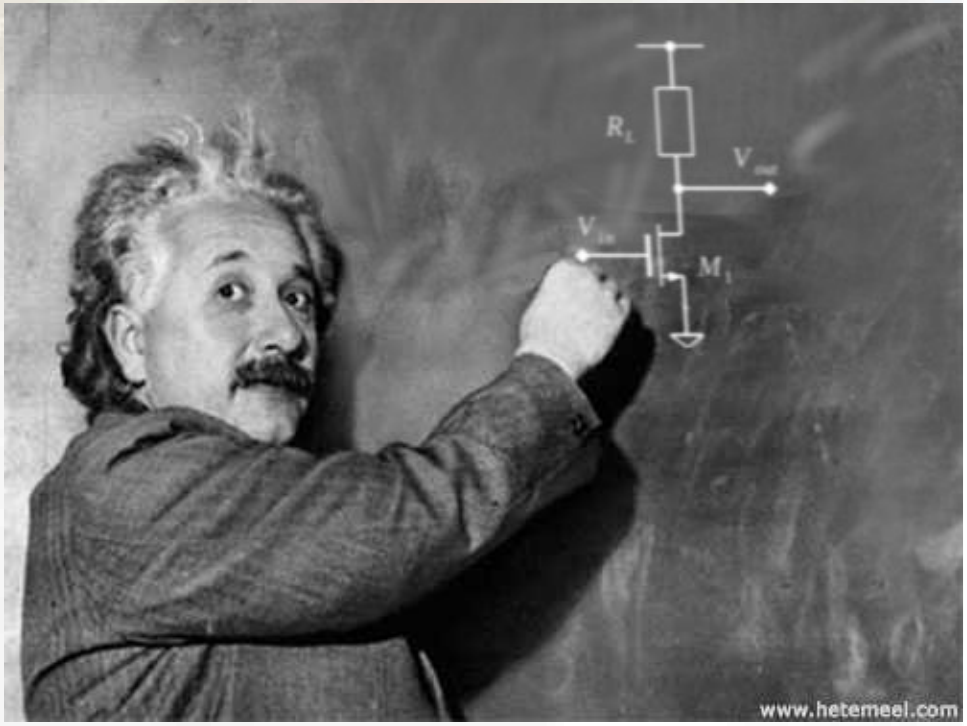
Open-loop vs. closed-loop gain

Bandwidth

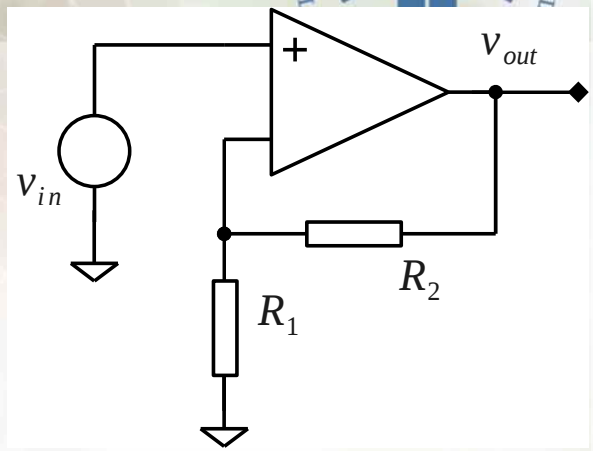
Speed of the closed loop

Offset error

Mismatch will cause an offset - how do we handle this?



Limited gain



Ideal case:

$$\frac{R_1}{R_1+R_2}\cdot v_{out}=v_{in}\Rightarrow\frac{v_{out}}{v_{in}}=\frac{R_1+R_2}{R_1}=\Gamma$$

Non-ideal gain case:

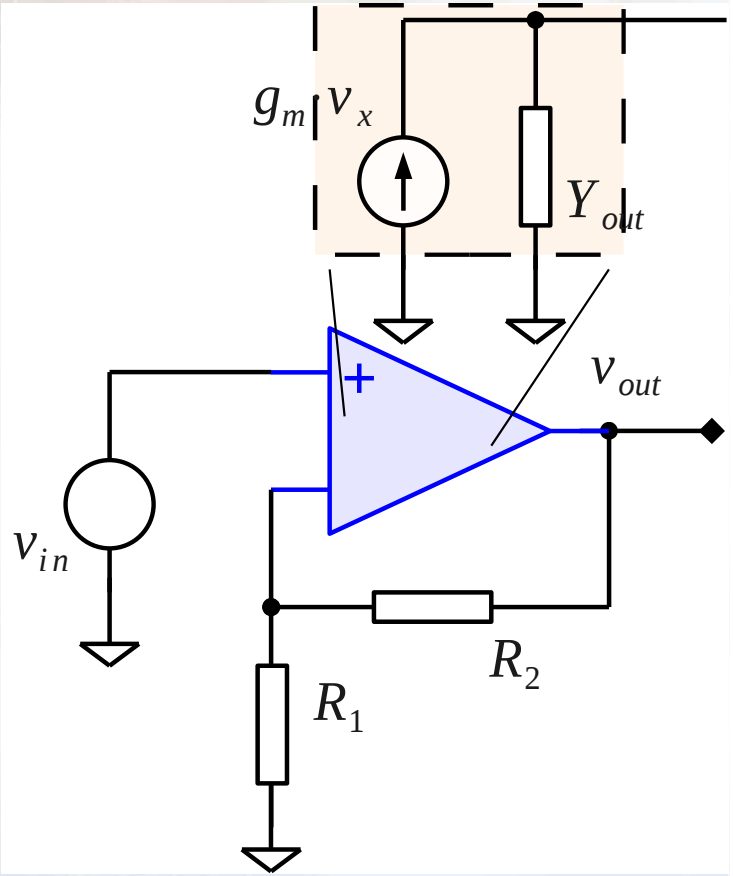
$$v_{out}=A_0\cdot\left[v_{in}-\frac{R_1}{R_1+R_2}\cdot v_{out}\right]\Rightarrow\frac{v_{out}}{v_{in}}=\frac{1}{\frac{1}{A_0}+\frac{R_1}{R_1+R_2}}=\;=\frac{R_1+R_2}{R_1}\cdot\frac{1}{1+\frac{R_1+R_2}{A_0\cdot R_1}}=\frac{\Gamma}{1+\frac{\Gamma}{A_0}}$$

Bandwidth

Single-pole (w/o output impedance)

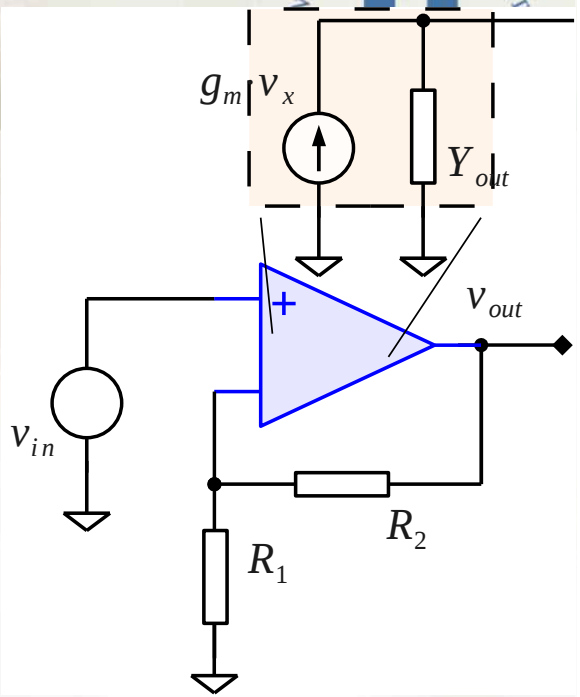
$$\frac{v_{out}}{v_{in}} = \frac{\Gamma}{1+\frac{\Gamma}{A_0}\cdot\left(1+\frac{s}{p_1}\right)}$$

$$\frac{v_{out}}{v_{in}} = \frac{\frac{\Gamma}{1+\Gamma/A_0}}{1+\frac{\Gamma/A_0}{1+\Gamma/A_0}\cdot\frac{s}{p_1}} \approx \frac{\Gamma}{1+\frac{s}{p_1\cdot A_0/\Gamma}}$$



The amplifier will band-limit the system!

More detailed model



$$v_x = \frac{R_1}{R_1 + R_2} \cdot v_{out}$$

$$g_m (v_{in} - v_x) + (0 - v_{out}) Y_{out} + \frac{0 - v_{out}}{R_1 + R_2} = 0$$

$$g_m v_{in} = v_{out} \cdot \left[Y_{out} + \frac{1 + R_1 g_m}{R_1 + R_2} \right]$$ and $$\frac{v_{out}}{v_{in}} = \frac{\Gamma}{1 + \frac{1}{g_m R_1} + \frac{\Gamma}{g_m / Y_{out}}}$$, etc., etc.

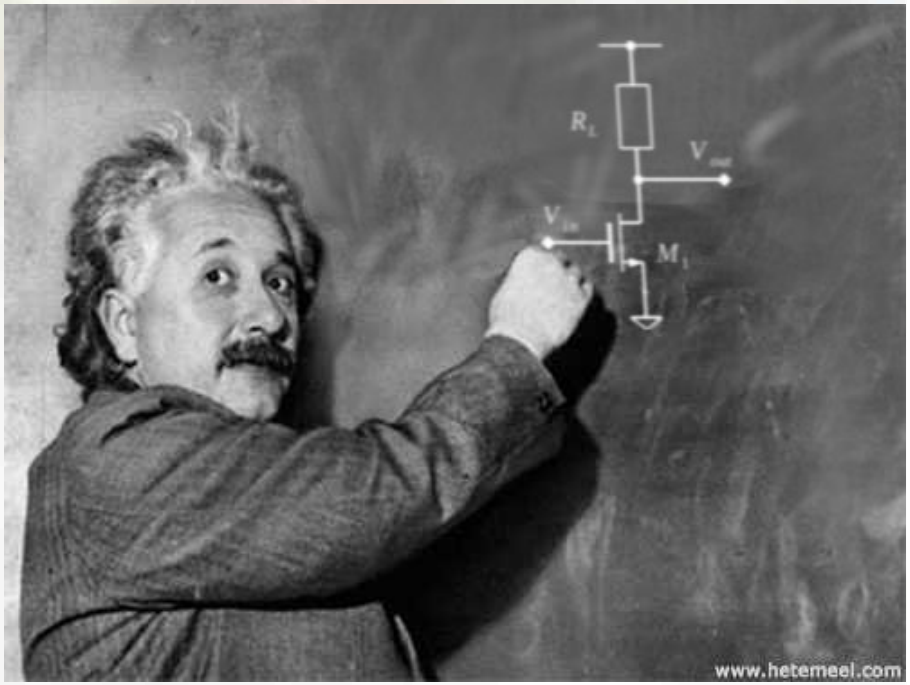
Other practical concerns wrt. current

Feedback with resistors

An OP given with a certain current drive capability will put requirements on the resistor sizes

What is the maximum swing?

What is the DC level?

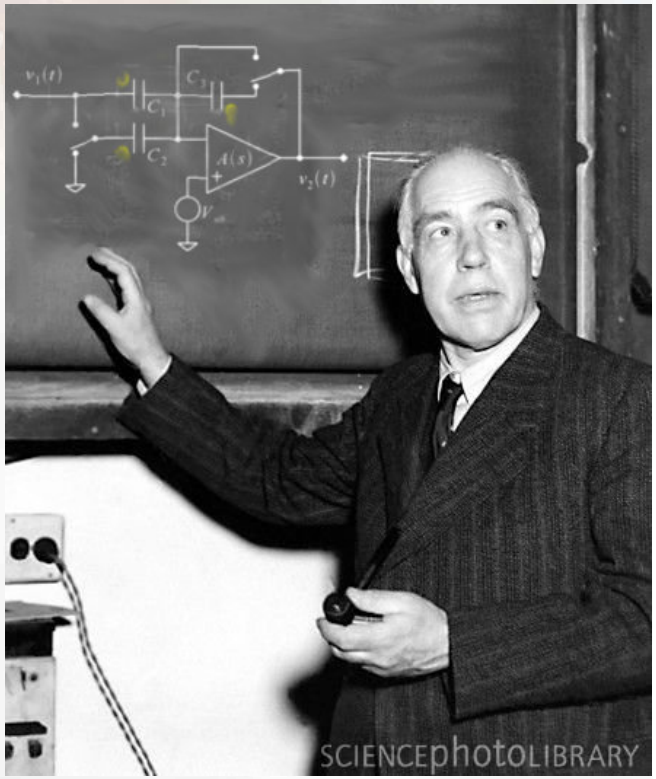


Other practical concerns wrt. gain

Integrator

Effect of limited gain on integration

operation. Maximum integration is A_0.



Low-pass filter

Effect on the filter bandwidth

How fast?

A closed-loop gain of 10 and a bandwidth of 25 MHz

The "741 amplifier"

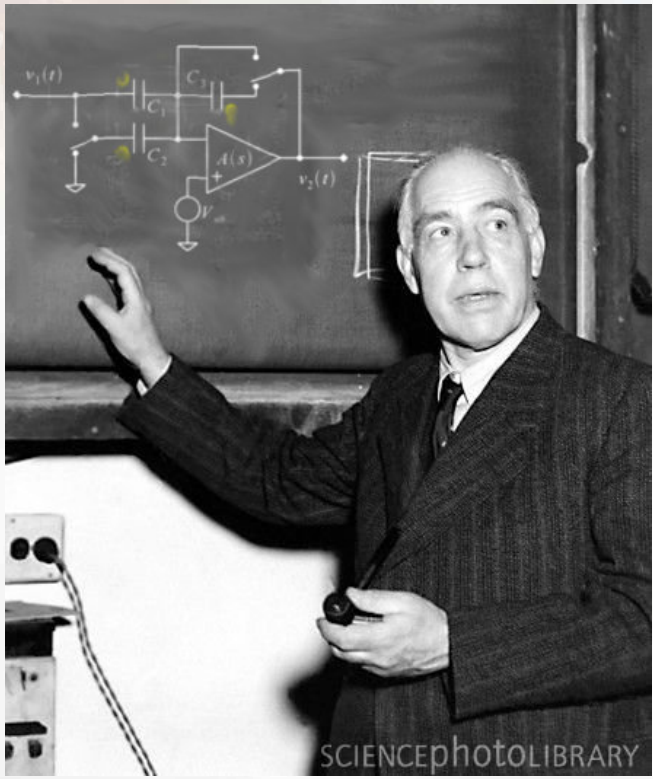
Texas instruments

opa 336 - what is the bandwidth?

opa 358 - what is the DC gain?

Analog Devices

AD854x - what is the DC gain, or what is the open-loop bandwidth?



Operational amplifier architectures

Left-overs

Examples

- Telescopic
- Two-stage
- Folded-cascode
- Current-mirror

Essentially just cascaded stages of different kinds

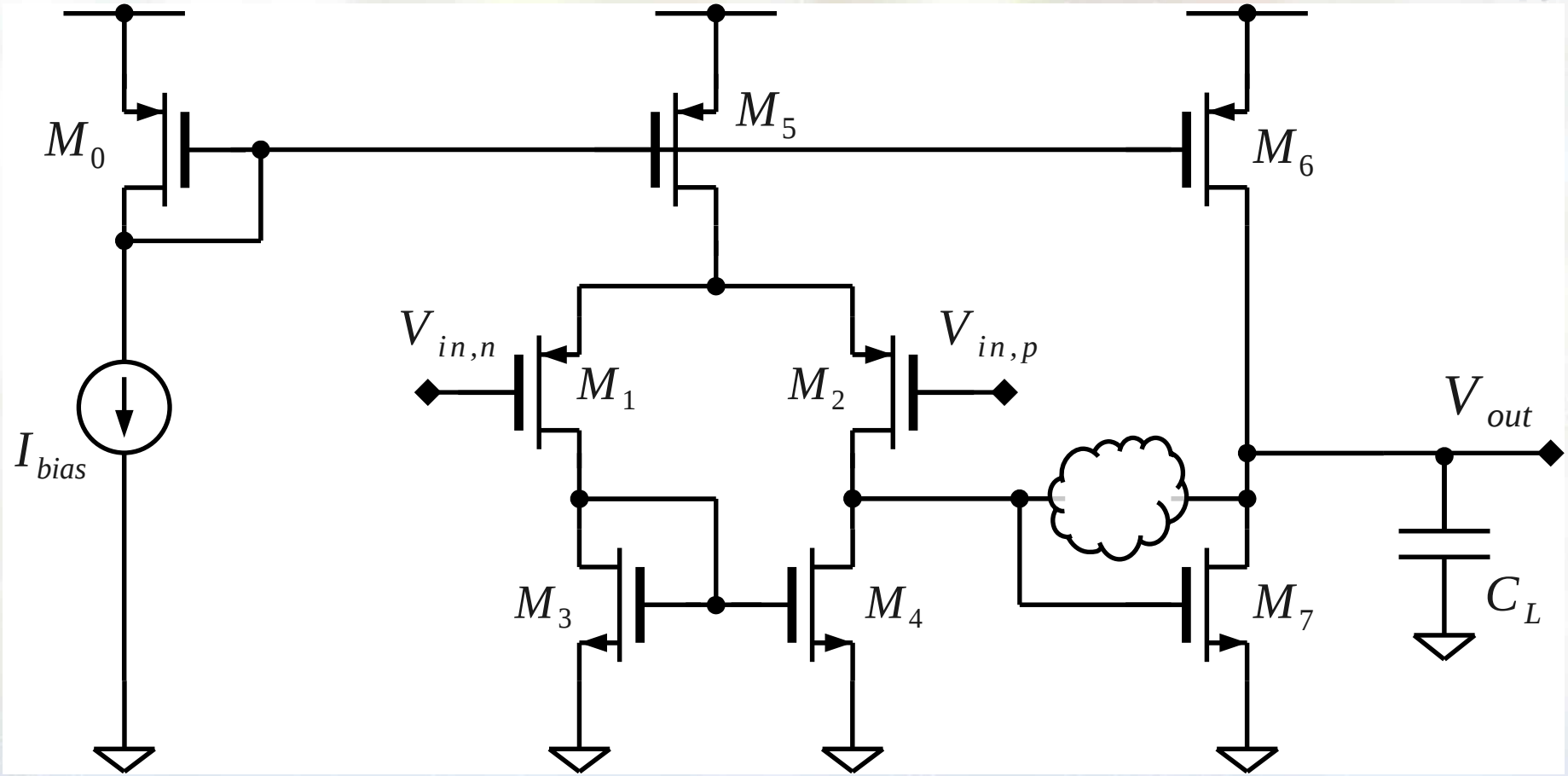
Telescopic OTA

Stack many cascodes on top of each-other. Use gain-boosting, etc.

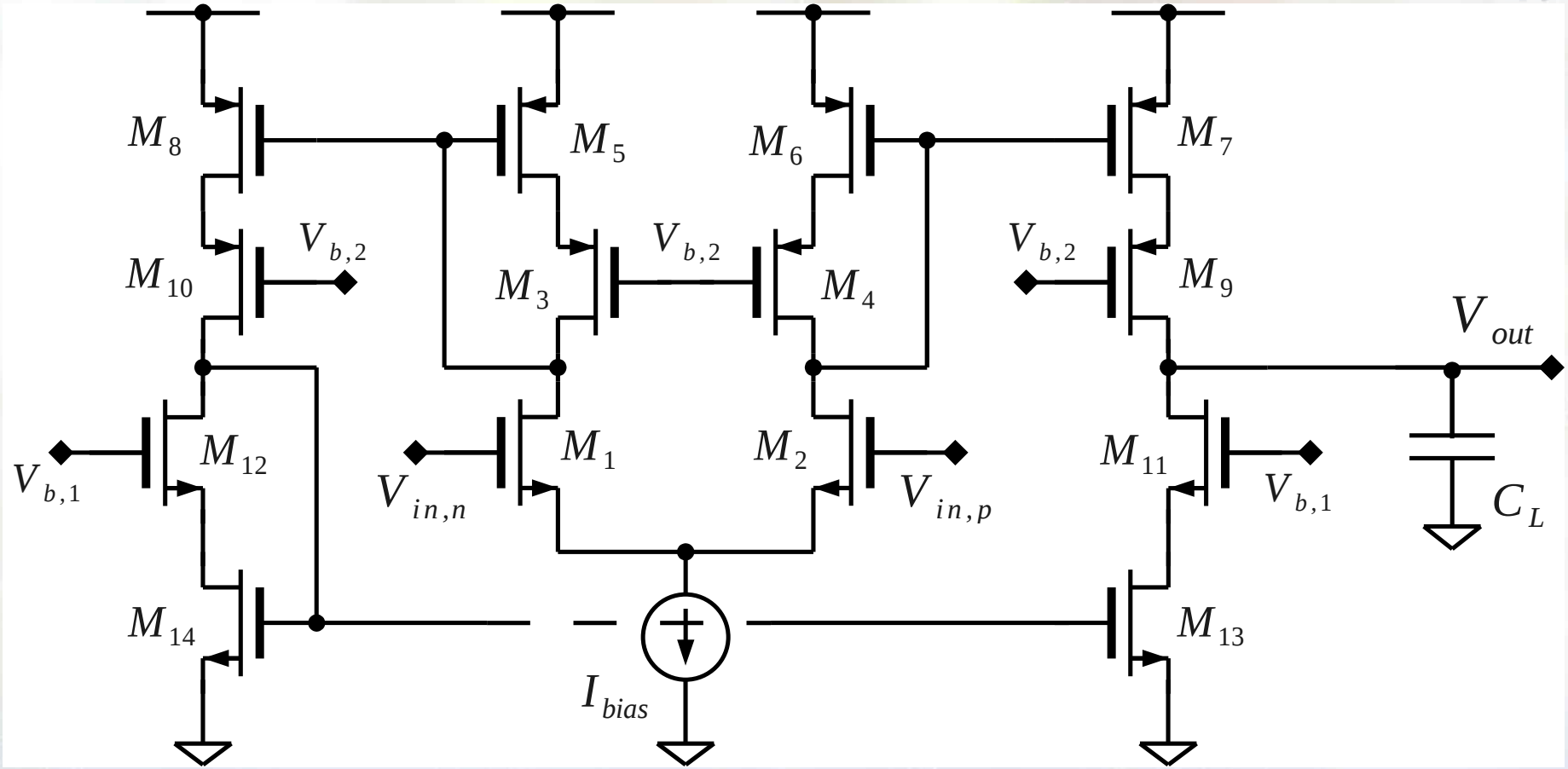
Omitted, since it is not applicable for modern processes.

The swing is eaten up.

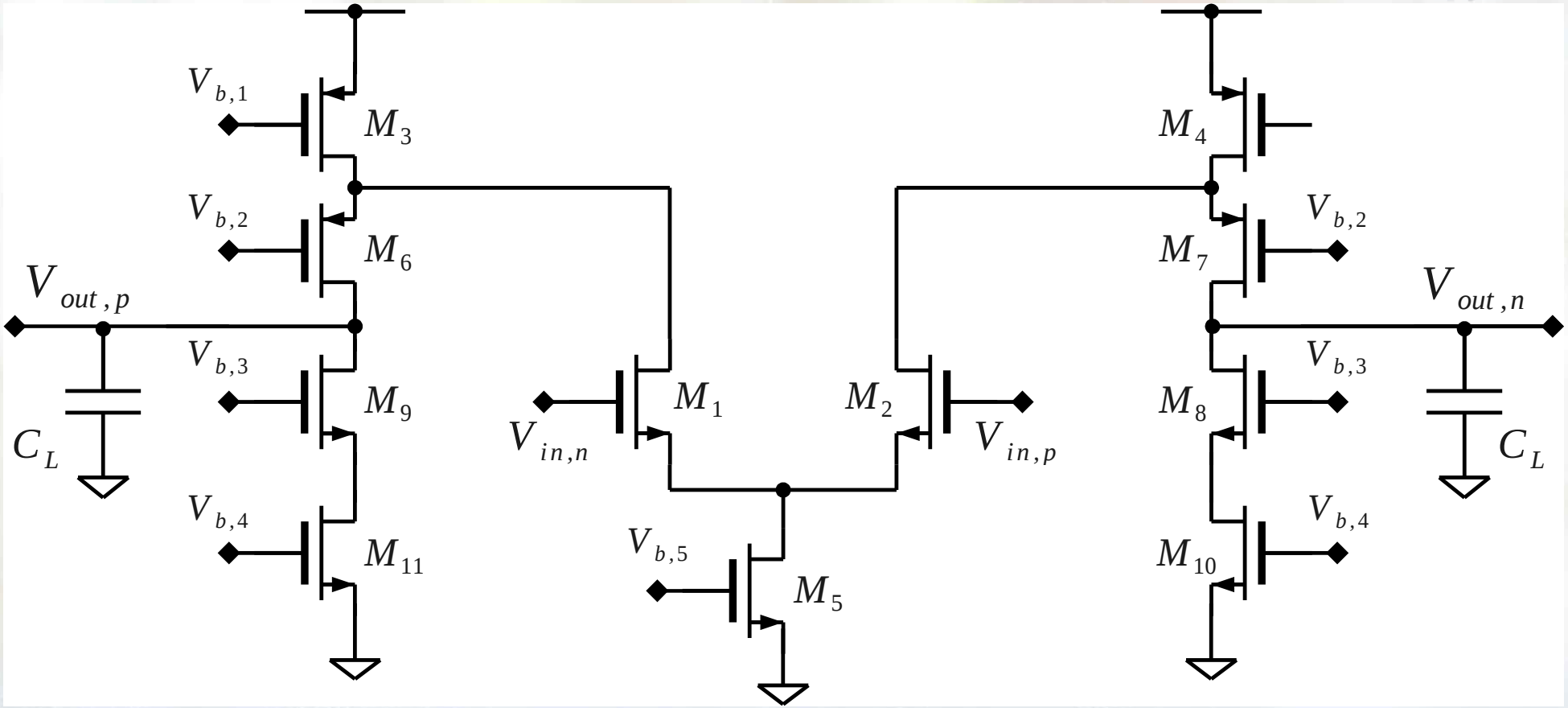
Two-stage OP/OTA



Current-mirror OP/OTA



Folded-cascode OP/OTA



OP/OTA Compilation, Cookbook recipes

Step-by-step explanation of OP/OTAs design

http://www.es.isy.liu.se/courses/ANDA/download/opampRef/ANTIK_0NNN_LN_opampHandsouts_A.pdf

Compensation techniques

http://www.es.isy.liu.se/courses/ANDA/download/opampRef/ANTIK_0NNN_LN_opampCompensationTable_A.pdf

Amplifier classes (inte i denna kurs)

Different classes, such as

Class A, B, AB, C, D, E, F, G, H, I, K, S, T, Z, etc.

Class A

Essentially the common-source stage

Class AB

Essentially a push-pull configured class A

Vad gjorde vi idag?

I princip blir vi klara med CMOS delen

Stabilitet och kompensering

Operationsförstärkaren

Vad står på tur nästa gång?

Distorsion

Linearitet

Brus

Fundamentala gränser på prestanda

Föreläsning 5, Brus och prestandamått

Noise and distortion

LiU EXPANDING REALITY

Vad gjorde vi förra gången?

Operational amplifiers

- Circuit-level aspects
- Simulation aspects
- Some terminology

Some practical concerns

- Limited current
- Limited bandwidth

Vad kommer vi göra idag?

Noise

- Circuit noise
- Thermal noise
- Flicker noise

Distortion

- What sets the (non)linearity in our CMOS devices?

Noise

Any circuit has noise and you, as a designer, have to reduce it or minimize the impact of it

"A disturbance, especially a random and persistent disturbance, that obscures or reduces the clarity of a signal."

Consequences

We need to use stochastic variables and power spectral densities, expectation values, etc.

We need to make certain assumptions (models) of our noise sources in order to calculate

Superfunction and spectral densitites

Power spectral density

Superfunction

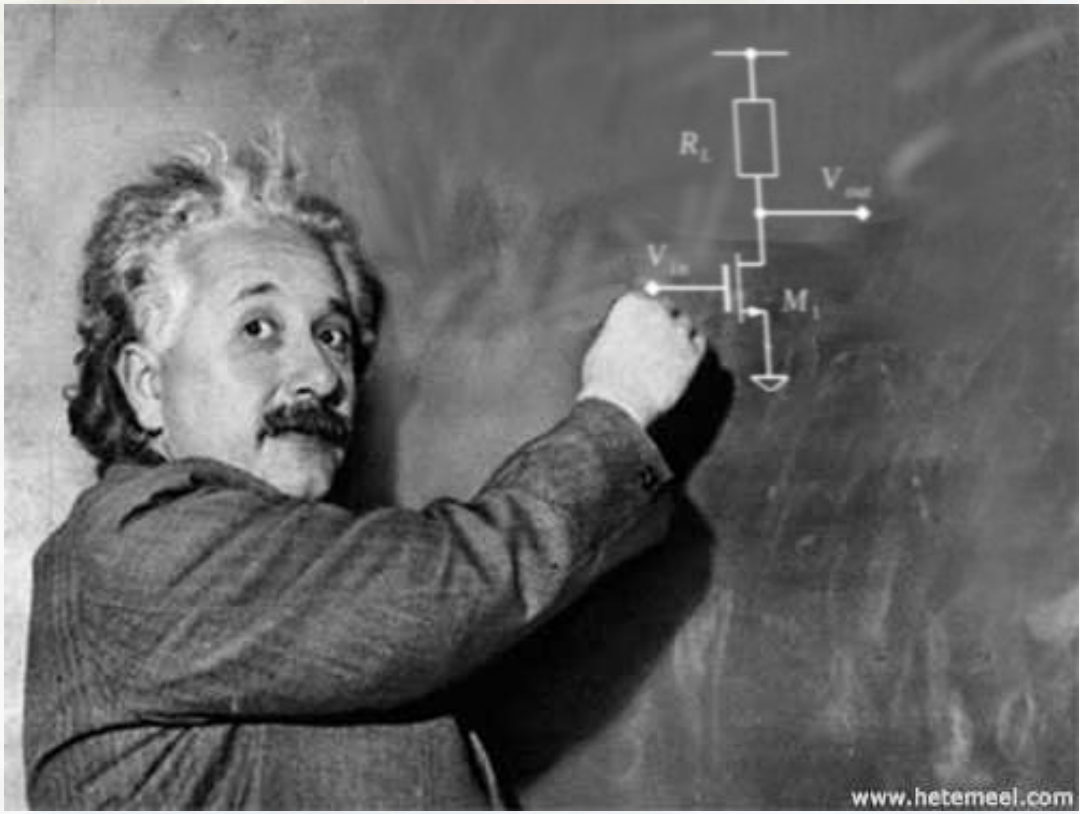
$$S_0(f) = \sum |A_i(f)|^2 \cdot S_i(f)$$

Total noise

$$V_{tot}^2 = \int v_n^2(f)\, df$$

Brickwall noise

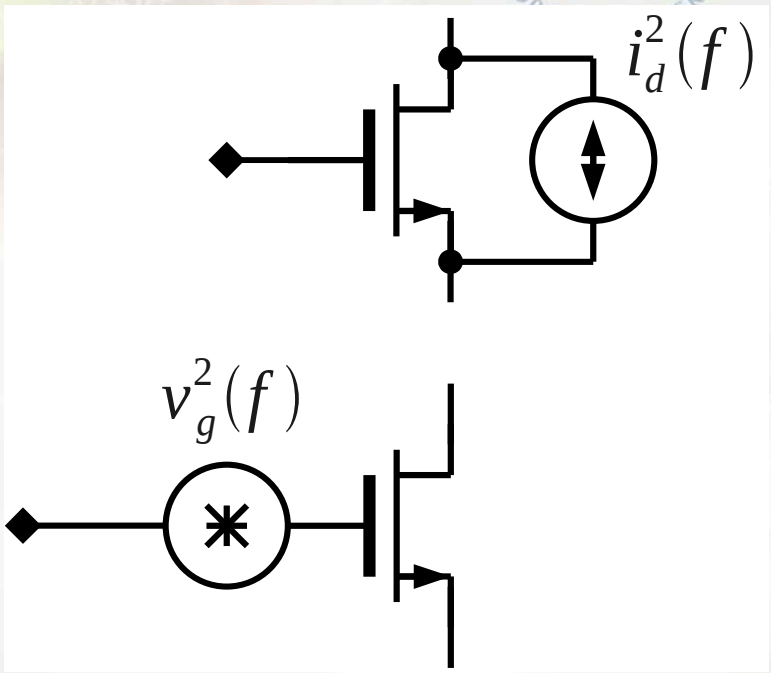
$$V_{tot}^2 = v_n^2(0) \cdot \frac{p_1}{4}$$



Thermal noise, white noise

Resistor

$$v_n^2 = 4kTR \quad \text{or} \quad i_n^2 = \frac{v_n^2}{R^2} = \frac{4kT}{R}$$



Transistor

$$v_g^2 = \frac{4kT\gamma}{g_m} \quad \text{or} \quad i_d^2 = v_g^2 \cdot g_m^2 = 4kT\gamma g_m$$

Opamp (återkommer vi till)

Flicker noise, 1/f-noise, pink noise

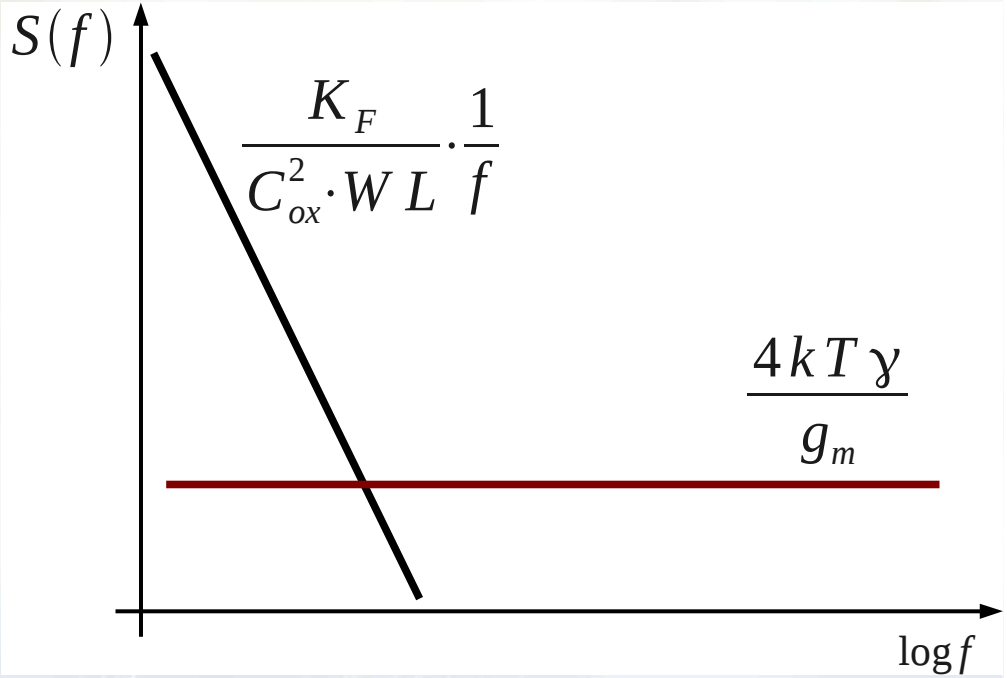
Resistor

$$v_n^2 = \frac{v_{bias}^2 \cdot k}{W\,L \cdot f} \text{ and } i_n^2 = R^2 \cdot v_n^2$$

Transistor

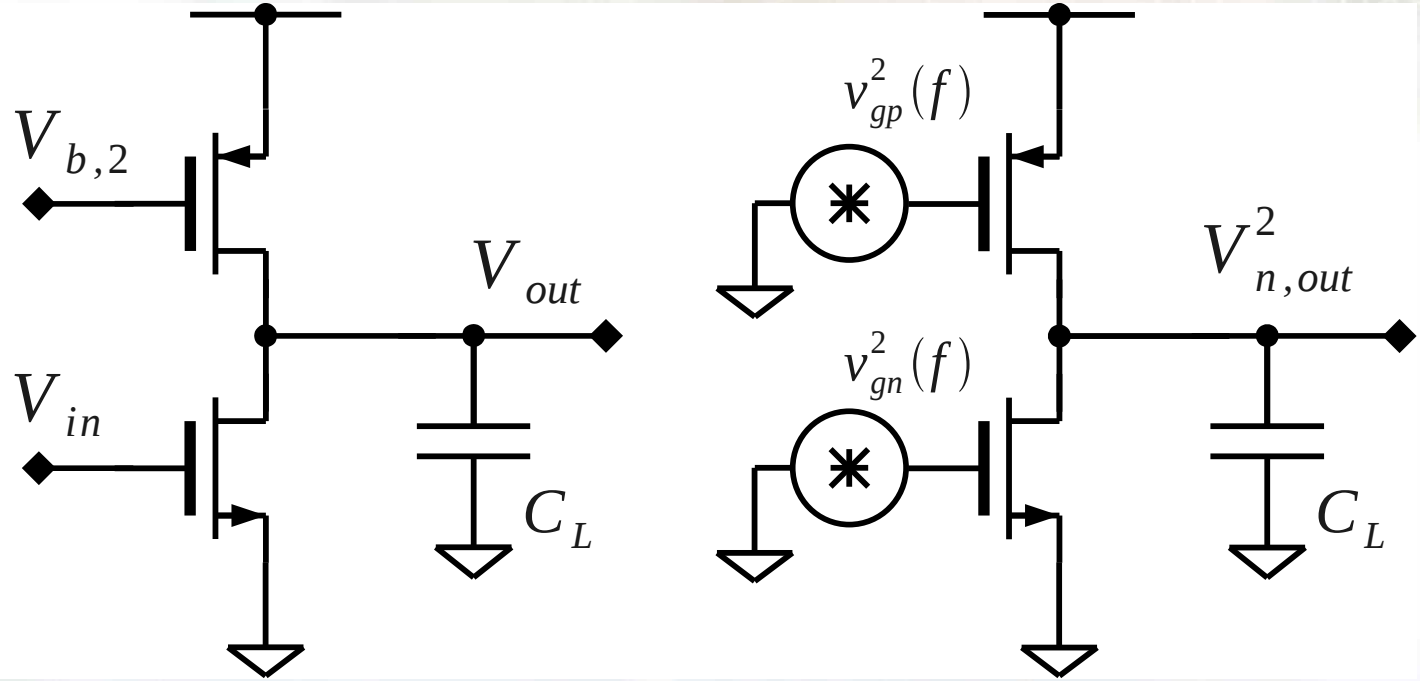
$$v_g^2 = \frac{K_F}{C_{ox}^2 \cdot W\,L} \cdot \frac{1}{f} \text{ and}$$

$$i_d^2 = g_m^2 \cdot v_n^2$$



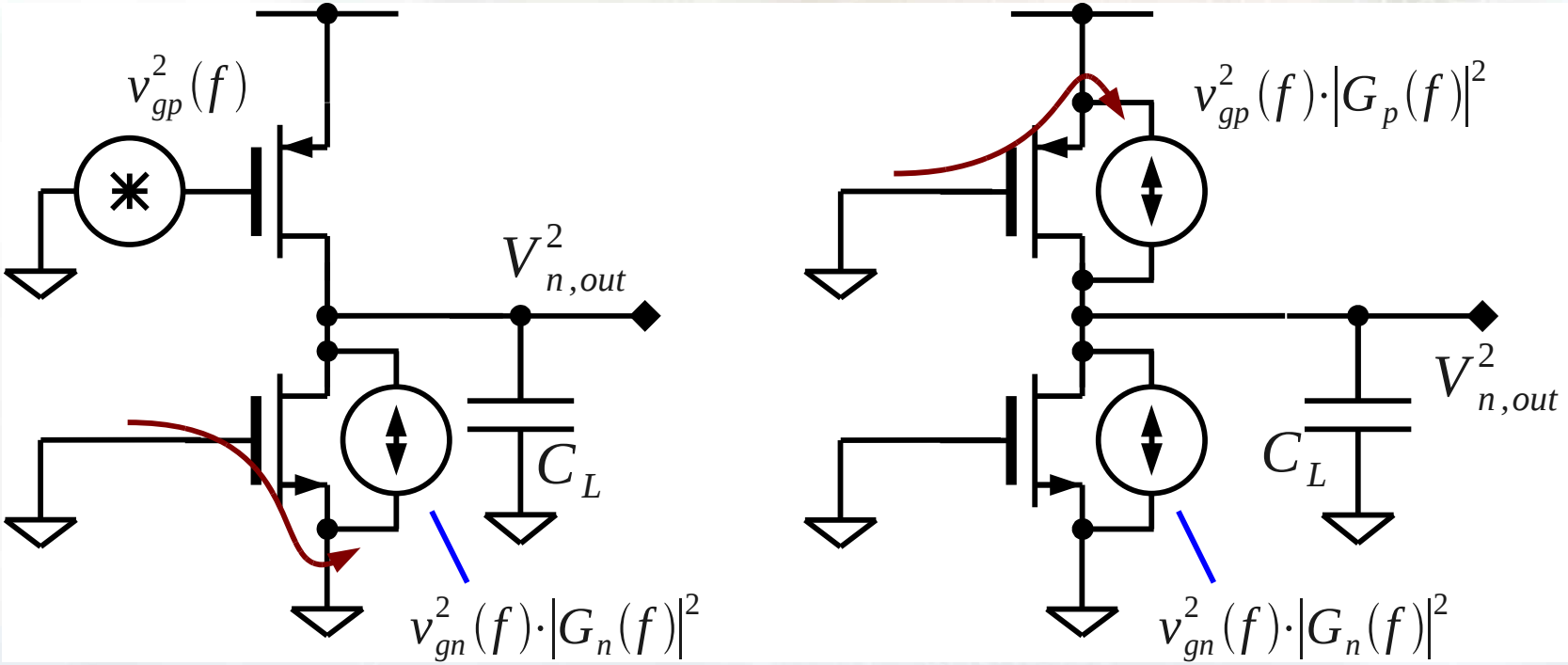
Noise compiled in one example

Common-source with noisy transistors



Noise compiled in one example, cont'd

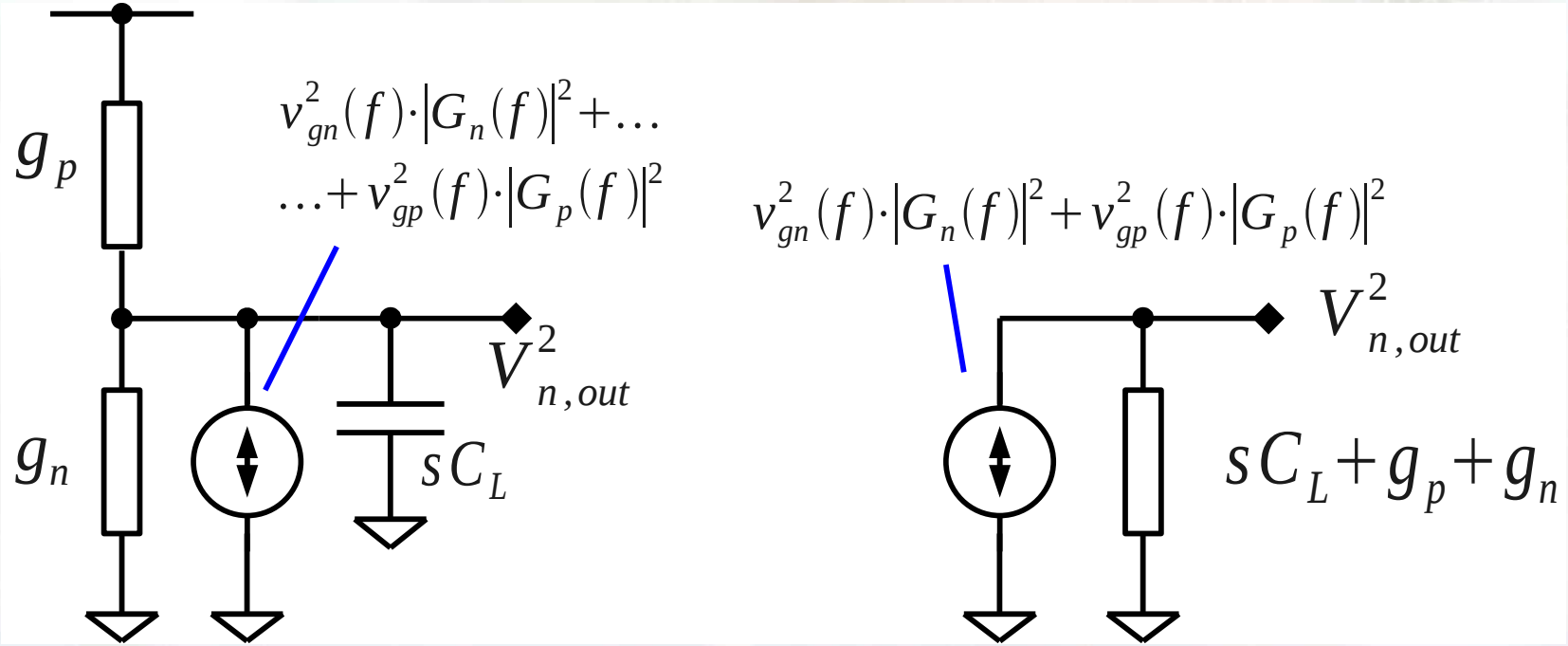
Potentially reorder the sources for convient calculations



Notice the use of transconductance from voltage to current.

Noise compiled in one example, cont'd

Equivalent small-signal schematics (ESSS)



Noise compiled in one example, cont'd

The general transfer function to the output is given by

$$V_{n,out}^2(f) = \frac{v_{gn}^2(f)\cdot|G_n(f)|^2 + v_{gp}^2(f)\cdot|G_p(f)|^2}{|sC_L + g_p + g_n|^2}$$

Insert the values

$$V_{n,out}^2(f) = 4kT\gamma\frac{\frac{g_{mn}^2}{g_{mn}} + \frac{g_{mp}^2}{g_{mp}}}{(g_p+g_n)^2\cdot\left|1+\frac{\frac{s}{g_p+g_n}}{C_L}\right|} = 4kT\gamma\frac{\frac{g_{mn}+g_{mp}}{(g_p+g_n)^2}}{\left|1+\frac{\frac{s}{g_p+g_n}}{C_L}\right|^2}$$

Noise compiled in one example, cont'd

$$V_{n,tot}^2 = \int V_{n,out}^2(f) = V_{n,out}^2(0) \cdot \frac{p_1}{4}$$

$$V_{n,tot}^2 = 4kT\gamma \frac{g_{mn}+g_{mp}}{(g_p+g_n)^2} \cdot \frac{g_p+g_n}{4C_L} = \frac{kT\gamma}{C_L} \cdot \frac{g_{mn}+g_{mp}}{g_p+g_n}$$

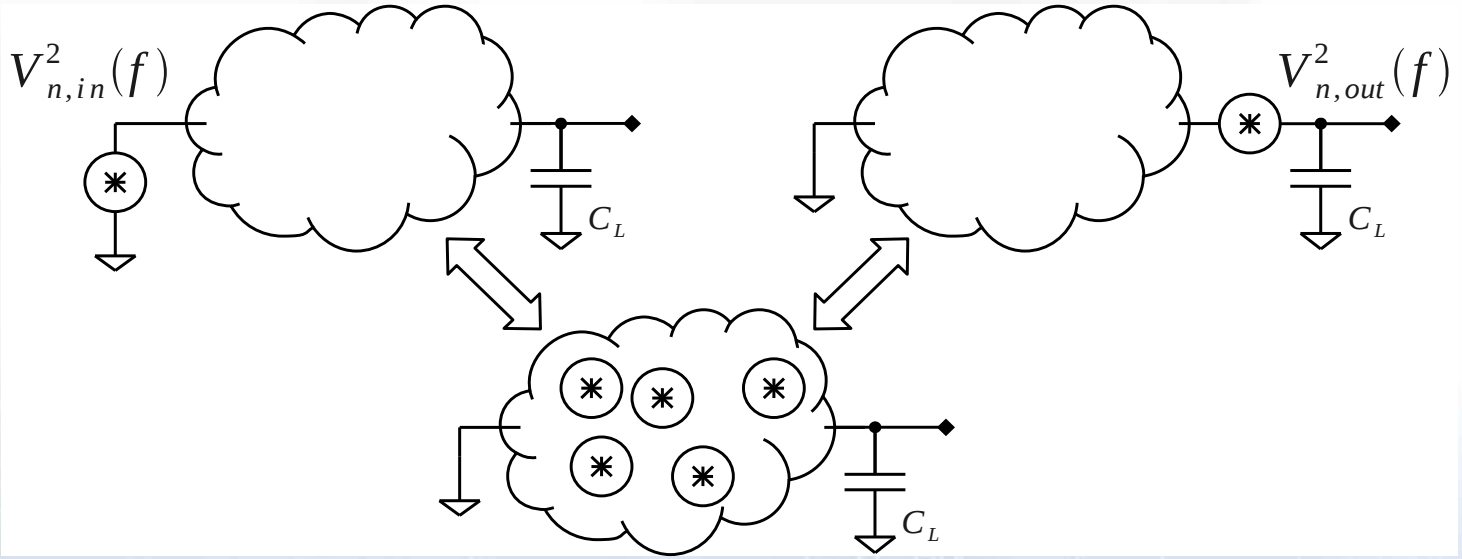
Conclude

$$V_{n,tot}^2 = \frac{kT\gamma}{C_L} \cdot A_0 \cdot \left(1 + \frac{g_{mp}}{g_{mn}}\right)$$

So called kT-over-C noise!

Input-referred noise

Revert the output noise back to the input: $$V_{n,in}^2(f) = \frac{V_{n,out}^2(f)}{|A_{in}(f)|^2}$$



The common-source example

Input-referred noise

$$V_{n,in}^2(f) = \left[4kT\gamma \frac{\frac{(g_{mn}+g_{mp})}{(g_p+g_n)^2}}{\left|1+\frac{s}{\frac{(g_p+g_n)}{C_L}}\right|^2} \right] \cdot \left[\frac{\left|1+\frac{s}{\frac{(g_p+g_n)}{C_L}}\right|^2}{\frac{g_{mn}^2}{(g_p+g_n)^2}} \right] = \frac{4kT\gamma}{g_{mn}} \cdot \left(1+\frac{g_{mp}}{g_{mn}} \right)$$

What does this mean?

Bias transistors should be made with low transconductance!

"Weak"

Gain should be made with high transconductance!

Not necessarily high voltage gain!

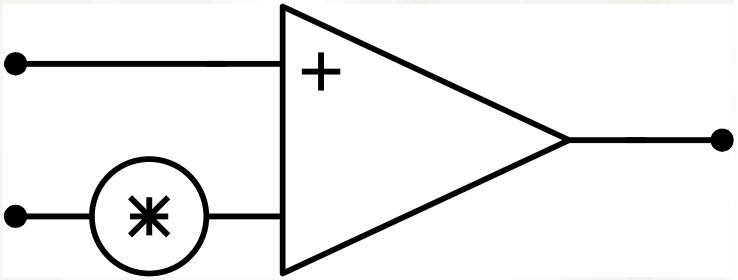
Gain should be distributed between multiple stages (Friis)

Left as an exercise

Noise in operational amplifiers

Opamps assumed to have input referred noise sources on its inputs

A voltage source



Two current sources

(Often ignored in CMOS opamps)

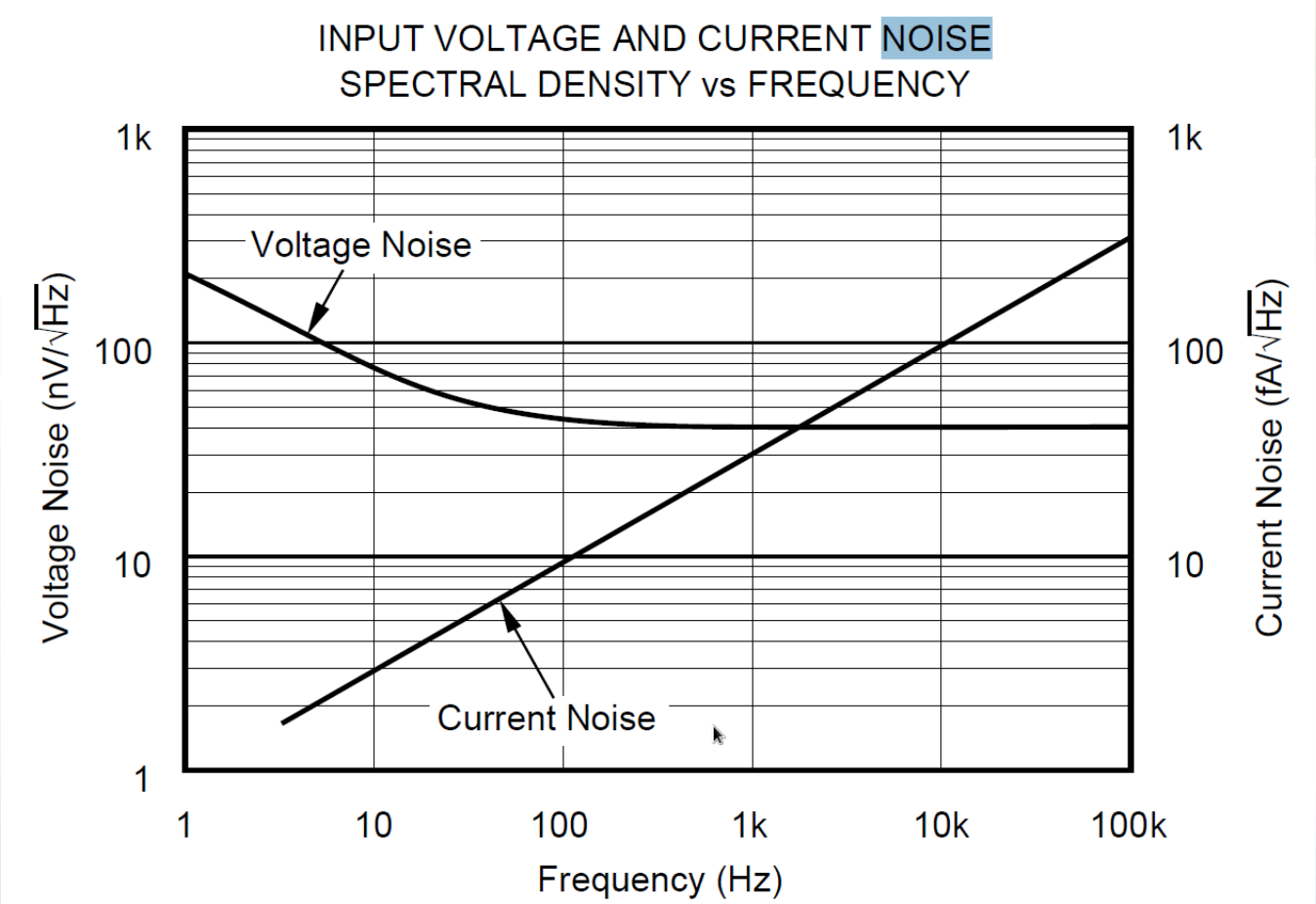
Input referred noise can be calculated according to previous principles and will be given by a spectral density

Example from "741" opamp

OPA336N (Texas Instruments)

Input Voltage Noise, f = 0.1 to 10 Hz	3 µVp-p
Input Voltage Noise Density, f = 1 kHz (e_n)	40 nV/√Hz
Current Noise Density, f = 1 kHz (i_n)	30 fA/√Hz

Example from "741" opamp



Noise in OP, example

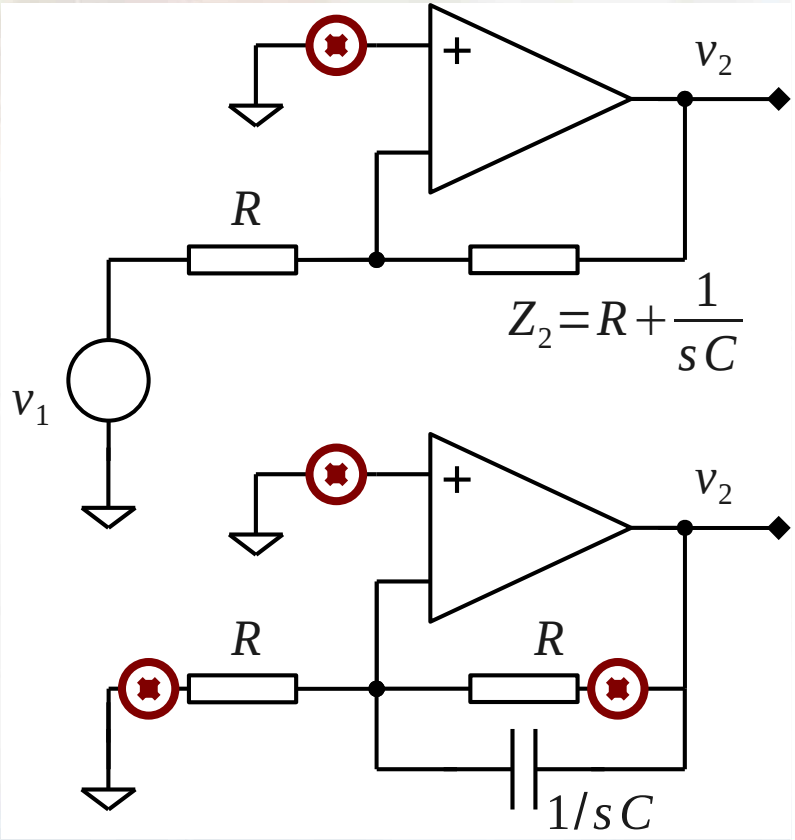
Noisy resistors and noisy opamp

$$\frac{V_2(s)}{V_1(s)} = \frac{-1}{1+sRC}$$

The noise sources, opamp

$$\frac{V_2(s)}{V_n(s)} = 1 + \frac{1}{1+sRC}$$

Ignore the current for now



Noise in OP, example cont'd

PSD

$$S_n(f) = \left| 1 + \frac{1}{1 + j\,2\pi f \cdot RC} \right|^2$$

A nasty transfer function - the noise never reaches zero!

Practically

The opamp unity-gain bandwidth will bandlimit the noise for which we can use the brickwall approach:

$$P_{tot,op} \approx 2 \cdot v_{n,op}^2(0) \cdot \frac{\omega_{ug}}{4}$$

Noise in OP, example cont'd

The noise sources, resistors

$$\frac{V_2(s)}{V_{r2}(s)}=\frac{1}{1+sRC} \text{ and } \frac{V_2(s)}{V_{r1}(s)}=\frac{-1}{1+sRC}$$

PSD

$$S_n(f)=\left|\frac{1}{1+ j2\pi f\cdot RC}\right|^2$$

A low-pass filter response - use the brickwall approach

$$P_{tot,R}\approx 2\cdot v_{n,R}^2(0)\cdot\frac{1/RC}{4}$$

Noise in OP, example cont'd

Combined

$$P_{tot} = P_{tot,R} + P_{tot,op} \approx 2 \cdot v_{n,op}^2(0) \cdot \frac{\omega_{ug}}{4} + 2\, v_{n,R}^2(0) \cdot \frac{1/RC}{4}$$

$$P_{tot} \approx v_{n,op}^2(0) \cdot \frac{\omega_{ug}}{2} + 4\,k\,T\,R \cdot \frac{1/RC}{2} = v_{n,op}^2(0) \cdot \frac{\omega_{ug}}{2} + \frac{2\,k\,T}{C}$$

This is the power normalized over 1 Ohm

$$v_{o,rms} = \sqrt{P_{tot}} \approx \sqrt{v_{n,op}^2(0) \cdot \frac{\omega_{ug}}{2} + \frac{2\,k\,T}{C}}$$

Noise in OP, example cont'd, values

Example:

$C=1$ nF, $R=10$ kOhm, i.e., a bandwidth of $f_{bw}\approx 14$-kHz

OPA336:

$v_{n,op}^2(0)\approx 1.6\cdot 10^{-15}$ sqV/Hz, and $f_{ug}\approx 100$ kHz

$$P_{tot}\approx 1.6\cdot 10^{-15}\cdot\frac{10^5}{2}+2\cdot\frac{4\cdot 10^{-21}}{10^{-9}}=88\cdot 10^{-12}$$

or $v_{o,rms}\approx 9.4$ uV

(compare with the reported 3 uV in the data sheet)

Signal-to-noise ratio (SNR)

At the output of our system, we will have a certain signal power. The signal-to-noise ratio (SNR) determines the quality of the system:

$$SNR = \frac{P_{sig}}{P_{noise}} \text{ or } SNR = 10 \cdot \log_{10}\left(\frac{P_{sig}}{P_{noise}}\right) \text{ or } SNR = 20 \cdot \log_{10}\left(\frac{v_{s,rms}}{v_{n,rms}}\right)$$

OPA336 example

Assume signal swing at output is $v_{rms} = 1$ V.

$$SNR \approx 20 \cdot \log_{10}\left(\frac{1}{9.4 \cdot 10^{-6}}\right) \approx 100 \text{ dB (approximately 16 bits)}$$

Distortion

Frequency-domain measures

- Spurious-free dynamic range, SFDR
- Harmonic distortion, HD
- Signal-to-noise-and-distortion ratio, SNDR

Amplitude domain measures

- Compression (clipping)
- Offset

Distortion

No circuit is linear...

$$Y = \alpha_0 + \alpha_1 \cdot X + \alpha_2 \cdot X^2 + \alpha_3 \cdot X^3 + \alpha_4 \cdot X^4 + \ldots$$

Example

$X = \sin \omega t$ is the sinusoidal, steady-state signal

$\alpha_1 = 1 , \alpha_2 = 0.01$ are characteristic coefficients of the system

Results in an output as

$$Y(t) = \sin \omega t + \alpha_2 \cdot \sin^2 \omega t = \sin \omega t + \alpha_2 \cdot \frac{1 - \cos 2 \omega t}{2}$$

Distortion, cont'd

Results in a DC shift and a distortion term

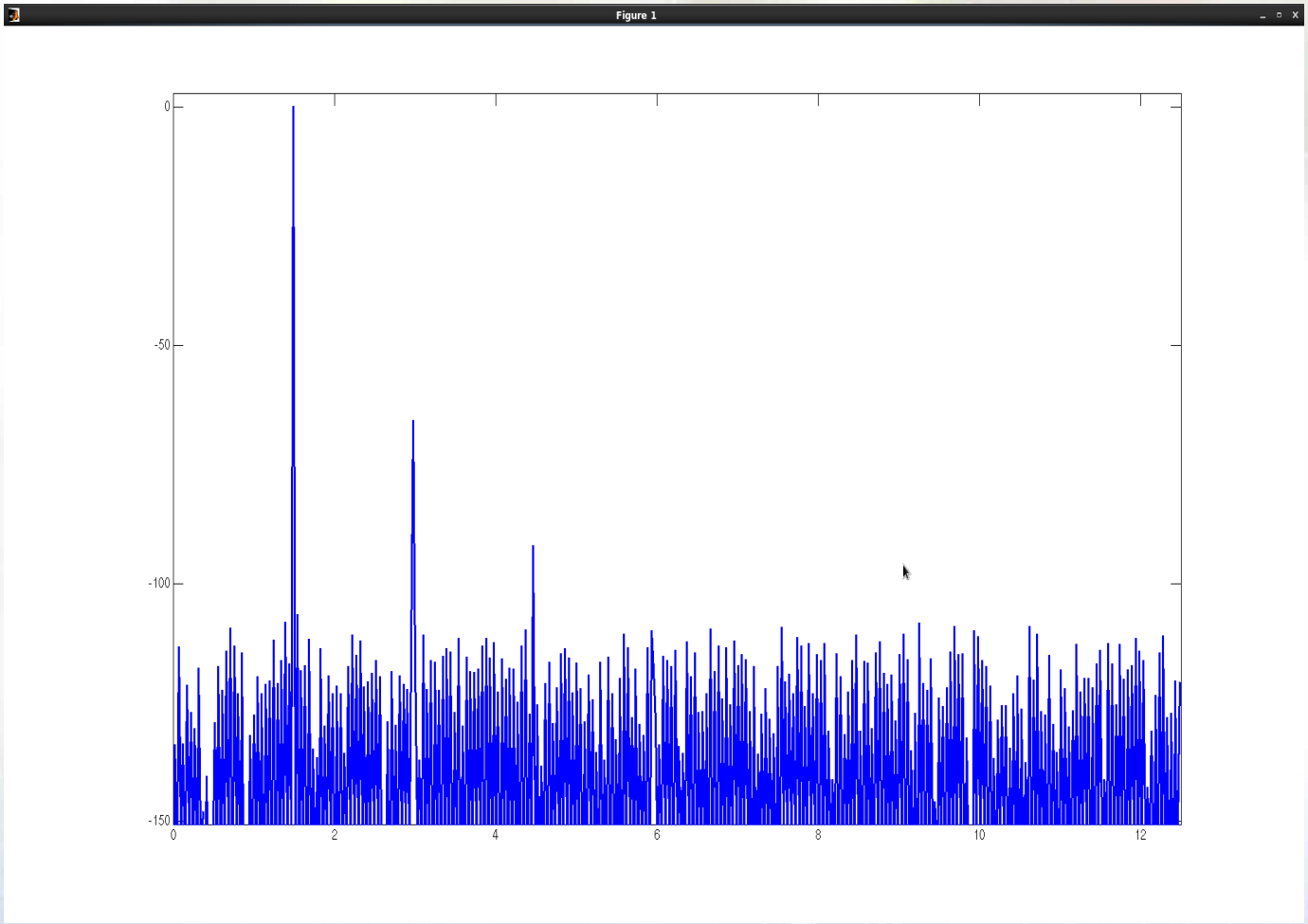
$$Y = \underbrace{\frac{\alpha_2}{2}}_{\text{DC shift}} + \underbrace{\sin \omega t}_{\text{desired}} - \underbrace{\frac{\alpha_2}{2} \cdot \cos 2\omega t}_{\text{distortion}}$$

Harmonic distortion

$$HD_2 = \frac{1^2}{(\alpha_2/2)^2} = \frac{1}{(0.01/2)^2} = 40000,$$

i.e., approximately 46 dB

Frequency domain measures



Distortion, fully differential circuits

Assume distortion is identical in two branches

$$Y_p = \alpha_0 + \alpha_1 \cdot X_p + \alpha_2 \cdot X_p^2 + \alpha_3 \cdot X_p^3 + \alpha_4 \cdot X_p^4 + \ldots$$ and

$$Y_n = \alpha_0 + \alpha_1 \cdot X_n + \alpha_2 \cdot X_n^2 + \alpha_3 \cdot X_n^3 + \alpha_4 \cdot X_n^4 + \ldots$$

Difference

$$\Delta Y = Y_p - Y_n = (\alpha_0 - \alpha_0) + \alpha_1 \cdot (X_p - X_n) + \alpha_2 \cdot \left(X_p^2 - X_n^2\right) + \ldots$$

Further on, assume input is already OK

$$X_p = -X_n = \frac{\Delta X}{2}$$

Distortion, fully differential, cont'd

Results in

$$\Delta Y = \alpha_1 \cdot (X_p - (-X_p)) + \alpha_2 \cdot \left(X_p^2 - (-X_p)^2\right) + \alpha_3 \cdot \left(X_p^3 - (-X_p)^3\right) + \ldots$$

and eventually

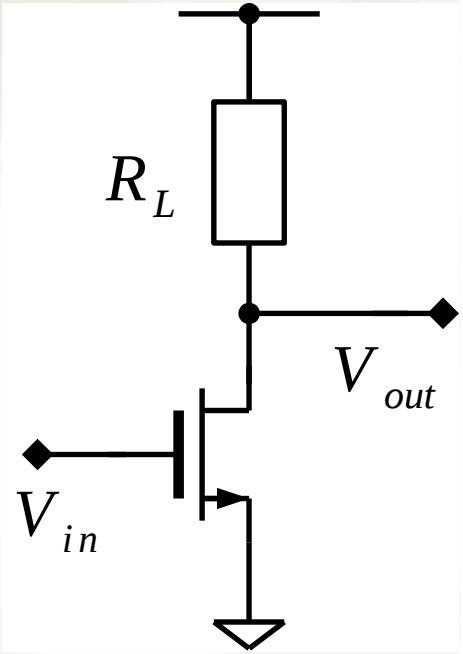
$$\Delta Y = \alpha_1 \cdot \Delta X + \frac{\alpha_3}{4} \cdot \Delta X^3 + \ldots$$

Even-order terms disappear!

Distortion in a common-source

Assume common-source stage resistive load

$I_D = \alpha \cdot V_{eff}^2$ och $V_{out} = V_{DD} - R \cdot I_D = V_{DD} - R \cdot \alpha \cdot V_{eff}^2$



Assume a limited input signal (no clipping)

$$V_{eff}(t) = V_{eff0} + V_x \cdot \sin \omega t$$

$$V_{out}(t) = V_{DD} - R \cdot \alpha \cdot \left(V_{eff0} + V_x \sin \omega t \right)^2$$

$$V_{out}(t) = V_{DD} - R \cdot \alpha \cdot \left(V_{eff0}^2 + 2 V_{eff0} V_x \cdot \sin \omega t + V_x^2 \cdot \sin^2 \omega t \right)$$

Continue to rewrite using trigonometrics

$$V_{out}(t) = V_{DD} - R \cdot \alpha \cdot \left(V_{eff0}^2 + 2 V_{eff0} V_x \cdot \sin \omega t + \frac{V_x^2}{2} \cdot (1 - \cos 2\omega t) \right)$$

$$V_{out}(t) = \underbrace{V_{DD} - R \cdot \alpha \cdot V_{eff0}^2 + \frac{V_x^2}{2}}_{\text{DC}} + \underbrace{2 V_{eff0} V_x \cdot R \cdot \alpha \cdot \sin \omega t}_{\text{desired signal}} - \underbrace{\frac{V_x^2}{2} \cdot \cos 2\omega t}_{\text{distortion}}$$

$$V_{out}(t) = \underbrace{V_{DD} - R \cdot \alpha \cdot V_{eff0}^2 + \frac{V_x^2}{2}}_{\text{DC}} + \underbrace{2 V_{eff0} V_x \cdot R \cdot \alpha \cdot \sin \omega t}_{\text{desired signal}} - \underbrace{\frac{V_x^2}{2} \cdot \cos 2\omega t}_{\text{distortion}}$$

Compression analysis

Signal power scales "linearly" with amplitude

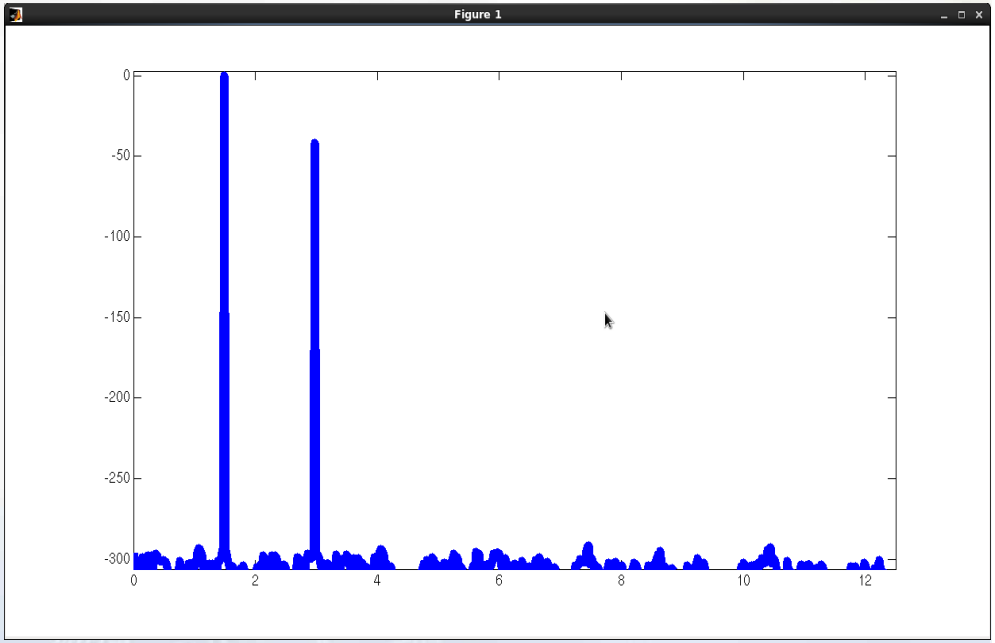
Distortion power scales "quadratically"

At some point they will meet.

Intercept points

Output and input-referred IIP, OIP

Common measures of nonlinearity



Distortion vs Noise, concludingly

High signal power gives high signal-to-noise ratio

High signal power gives low signal-to-distortion ratio

This means that you need to distribute the gain between the different stages accordingly and trade-off between the two.

Vad gjorde vi idag?

Noise

Circuit noise

Thermal noise

Flicker noise

Distortion

What sets the (non)linearity in our CMOS devices?

Vad står på tur nästa gång?

PCB vs silicon

What are the differences when scaling up the geometries

Components

Surface-mounted components

PCB

Some PCB specifics

Föreläsning 6, Filtrering, AD/DA

Dataomvandlare och kort kommentar om filter

LiU EXPANDING REALITY

Vad gjorde vi förra gången?

Brus och prestandamått

Brusbandbredd

Distortion

Vad kommer vi göra idag?

Filters

A quick view of filters for an analog signal chain

Data converters (dependent on time, might be pushed out to next lecture)

An overview of data converters
An understanding of the frequency domain

The oversampling data converter

Analoga filter

Linear, frequency-selective filter

Different types of filters

Band-select filters (for telecom and noise reduction)
Anti-aliasing filters (for the ADC)
Reconstruction filters (for the DAC)
Notch filters (for disturbances at specific frequencies)

Effectively realizing an LTI transfer function

$$H(s) = H_0 \cdot \frac{a_N \cdot s^N + \ldots + a_1 \cdot s + a_0}{b_M \cdot s^M + \ldots + b_1 \cdot s + b_0}$$

Analog filters, cont'd

A general transfer function for a linear system is given by

$$H(s)=\frac{Y(s)}{X(s)}=\frac{a_0+a_1 s+a_2 s^2+\ldots}{b_0+b_1 s+b_2 s^2+\ldots}$$

$$Y(s)\cdot\left(b_0+b_1 s+b_2 s^2+\ldots\right)=X(s)\cdot\left(a_0+a_1 s+a_2 s^2+\ldots\right)$$

$$Y(s)=X(s)\cdot\left(\alpha_0+\alpha_1\frac{1}{s}+\alpha_2\frac{1}{s^2}+\ldots\right)-Y(s)\cdot\left(\beta_1\frac{1}{s}+\beta_2\frac{1}{s^2}+\ldots\right)$$

Create a “recursive” set of integrations

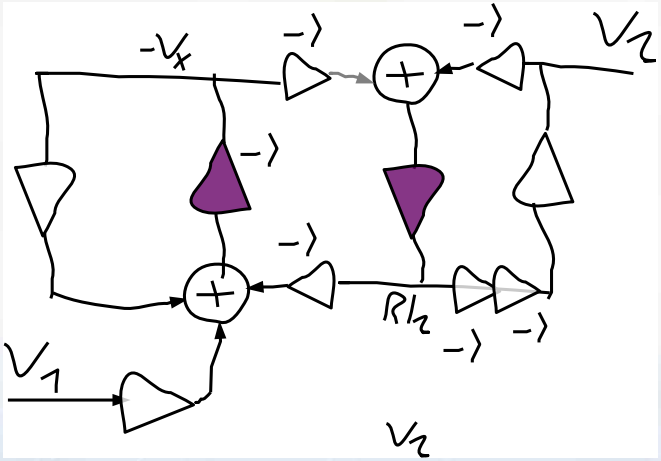
$$Y(s)=\alpha_0\cdot X(s)+\frac{1}{s}\cdot\left(\alpha_1 X(s)-\beta_1\cdot Y(s)+\frac{1}{s}\cdot\left(\alpha_2\cdot X(s)-\beta_2\cdot Y(s)+\frac{1}{s}\cdot(\ldots)\right)\right)$$

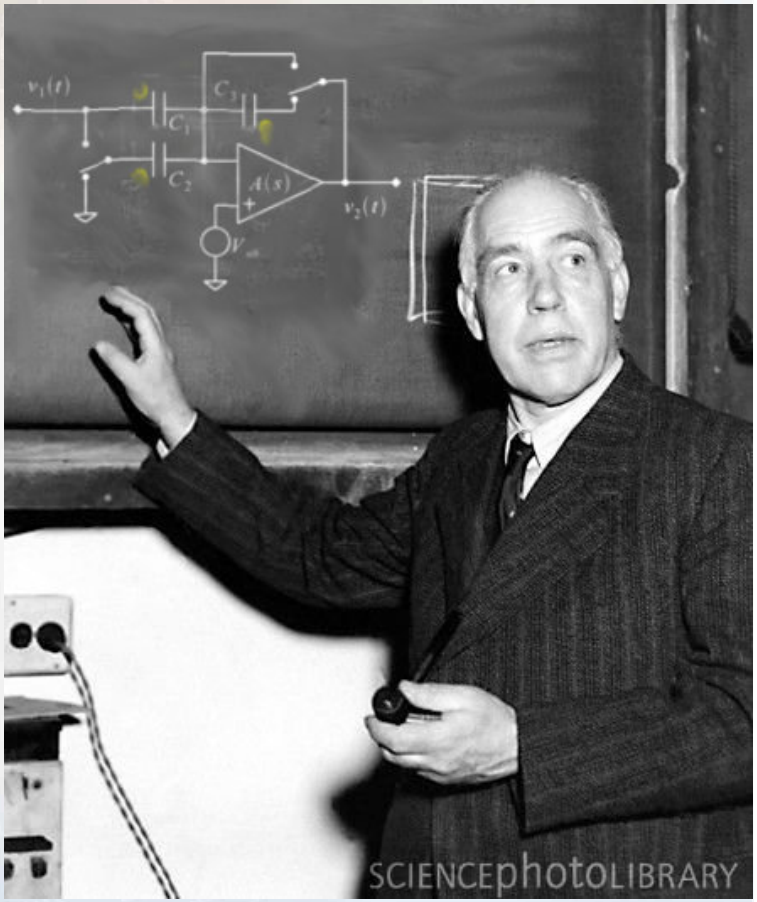
Continuous-time filters, flow graph

Manipulation

Replacing with integrators

Feedback, etc.





Cascading of several stages

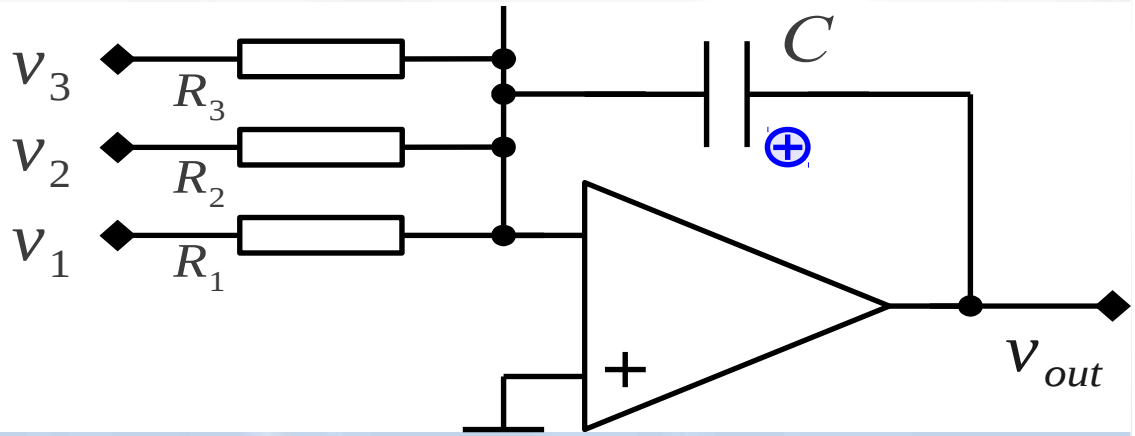
Active-RC

Summation of different inputs is done with the resistors, i.e., we are summing up the currents in the virtual ground node:

$$-V_{out}(s)\cdot s\,C_L = I_1(s) + I_2(s) + I_3(s) = \frac{V_1(s)}{R_1} + \frac{V_2(s)}{R_2} + \dots$$

Which combined gives us the integration

$$V_{out}(s) = -\frac{V_1(s)}{s\,C_L R_1} - \frac{V_2(s)}{s\,C_L R_2} + \dots$$



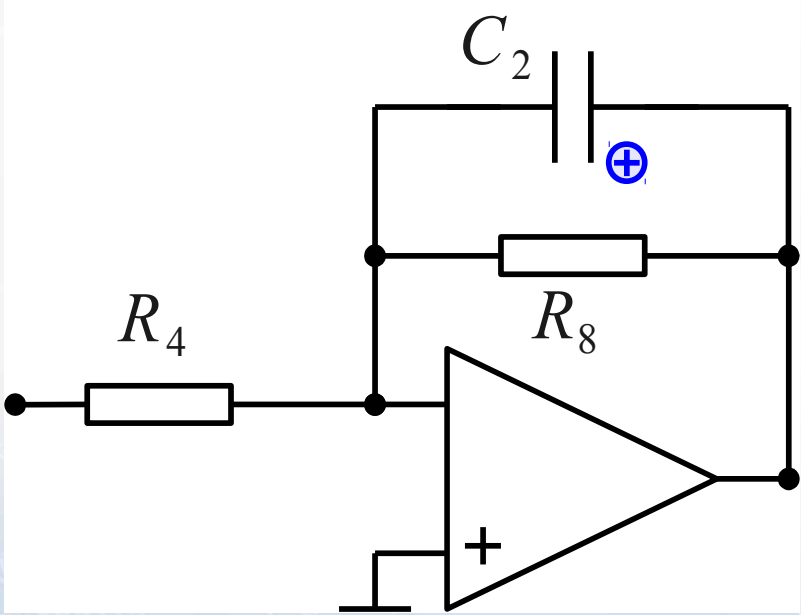
Example, first-order pole with active-RC

Sum the currents in the virtual ground:

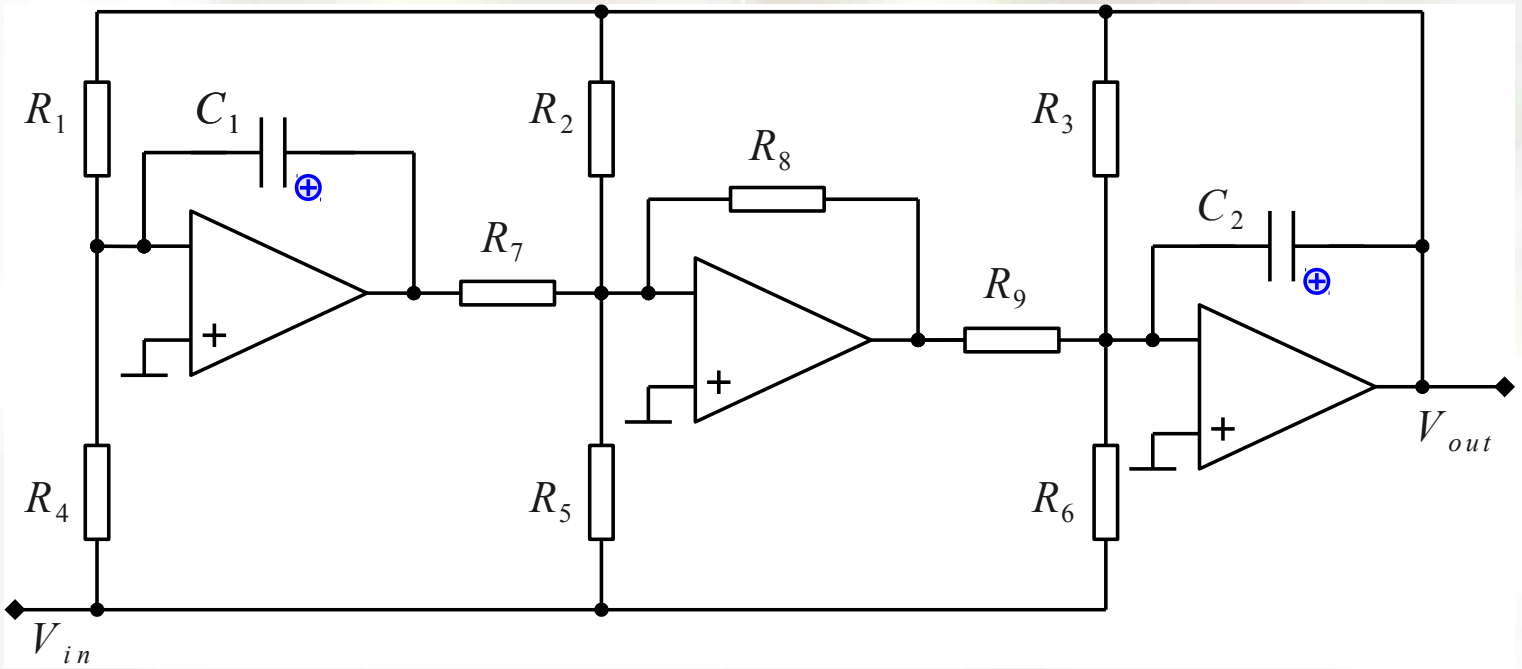
$$V_{out}(s)\cdot s\,C_2 = \frac{-V_{in}(s)}{R_4} - \frac{V_{out}(s)}{R_8}$$

such that

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{-R_8/R_4}{1+\frac{s}{1/C_2 R_4}}$$



Example: Tow-Thomas, Biquad, and more, ...



Output isolated and buffered with OP

Single-pole formed with single RC at output or input

Analog filters, Architectures

Ideally

Best performance is obtained with a leapfrog or ladder filter.
Less sensitive to component variations

Practically

Select a set of cascaded stages on the board instead.

Design for one extra pole whenever possible (two poles /OP)

Quite a few software tools "out there" that provide you with the values once you know the specification.

Off-the shelf integrated analog circuits with filtering options

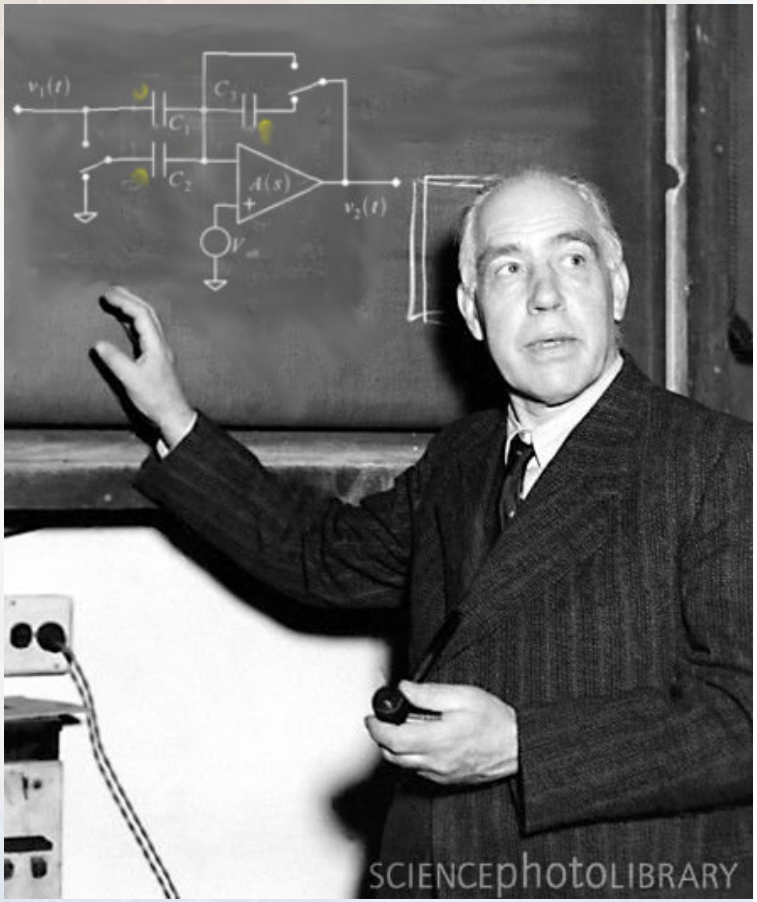
Analog filters, Architectures, cont'd

Comparison

Two lowpass filters with same, but different, properties.

Scaling

Scale your signal levels to maximize the input/output range.



Analog filters, opamp considerations

Speed

Unity-gain frequency of the opamp should be considerably larger than the closed-loop gain times the cut-off frequency

$$f_{ug} > 100 \cdot A_{CL} \cdot f_{bw}$$ (example)

Current drive capability

Slew rate must cope with the highest frequency of your filter:

$$|\mathrm{SR}| > 2\pi \cdot f_{bw} \cdot V_{out,pp}$$ (assuming sinusoid signal)

Noise, limited gain we have discussed in previous lectures

Data converters fundamentals

DAC

Represents a digital signal with an analog signal
To control something
To transmit something (a modulated signal)

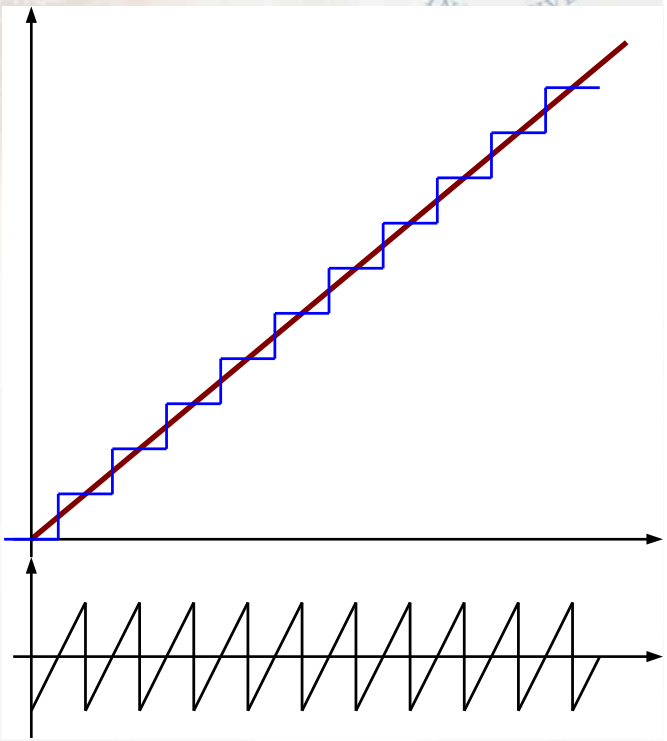
ADC

Represents an analog signal with a digital signal
To measure something
To receive something (a modulated signal)

The quantization process

Only distinct levels represented

Error is the deviation from straight line



A range from 0 to V_{ref} gives the LSB step

$$\Delta = \frac{V_{ref}}{2^N}$$

The quantization error is bound

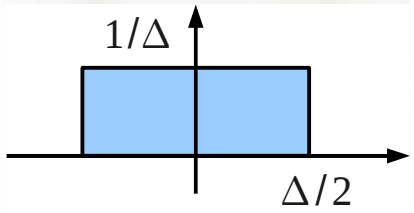
$$Q \in \left\{ -\frac{\Delta}{2}, \frac{\Delta}{2} \right\}$$

Quantization process, cont'd

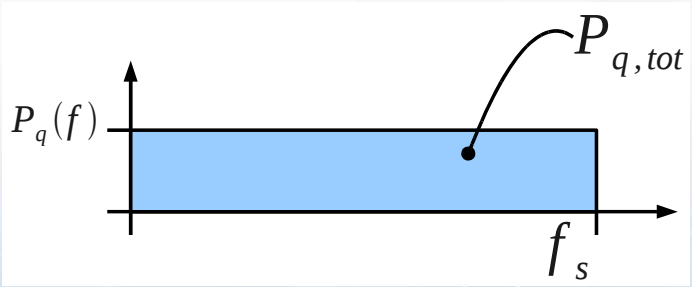
Assume signal-independent (not true for low number of bits)

Quantization assumed to be a stochastic process

White noise, uniformly distributed in $\left\{-\frac{\Delta}{2}, \frac{\Delta}{2}\right\}$



Noise power spectral density



Quantization process, cont'd

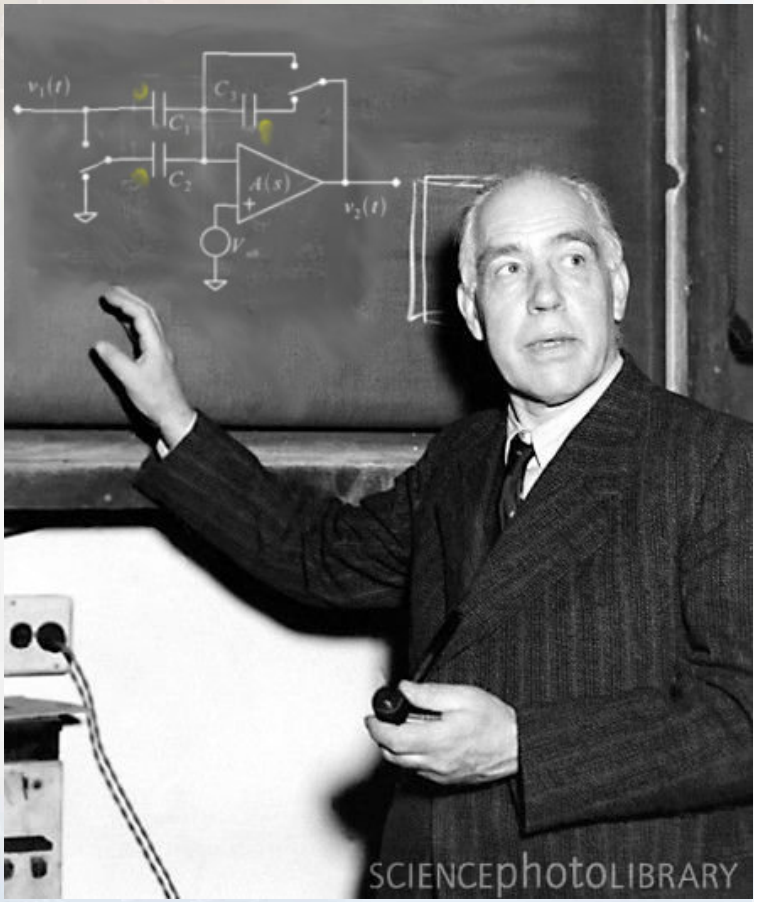
Sigma of the probabilistic noise

Noise model

Remember the superfunction

Power spectral density

A certain bandwidth contains a certain amount of noise



The quantization process, cont'd

Peak power assuming centered around the nominal DC level

$$P_{pk} = \left(\frac{V_{ref}}{2} \right)^2$$

Maximum, average sinusoidal power

$$P_{avg} = \frac{1}{2} \cdot \left(\frac{V_{ref}}{2} \right)^2 = \frac{1}{8} \cdot V_{ref}^2 = \frac{P_{pk}}{2}$$

Peak-to-average ratio (PAR) for a sinusoid

$$\mathrm{PAR} = \frac{P_{pk}}{P_{avg}} = 2 \ (1.76 \text{ dB})$$

The quantization process, cont'd

Noise power given by the sigma: $P_{q,tot} = \sigma^2 = \Delta^2/12$

Signal-to-quantization-noise ratio: $\mathrm{SQNR} = \frac{P_{avg}}{P_{q,tot}} = \frac{P_{pk}}{P_{q,tot} \cdot \mathrm{PAR}}$

With values inserted

$$\mathrm{SQNR} = \frac{V_{ref}^2/4}{\frac{1}{12} \cdot \left(\frac{V_{ref}}{2^N}\right)^2 \cdot \mathrm{PAR}} = \frac{3 \cdot 2^{2N}}{\mathrm{PAR}}$$

or in a logarithmic scale:

$\mathrm{SQNR} \approx 6.02 \cdot N + 4.77 - \mathrm{PAR} = 6.02 \cdot N + 1.76$ for our sinusoid.

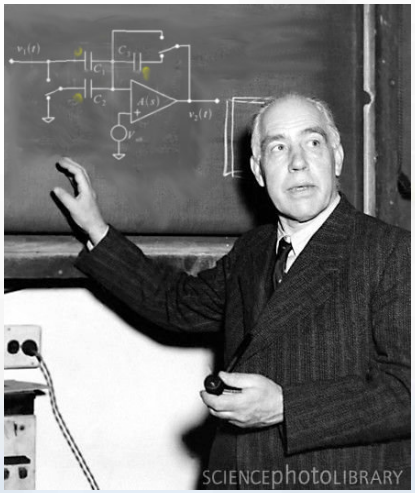
D/A conversion as such

Amplitude is generated by scaling the digital bits and summing them

$$A_{out}(nT) = \sum_{k=0}^{N-1} w_k(nT) \cdot 2^k$$

The scaling does not necessarily have to be binary:

Binary, Thermometer, Linear, Segmented



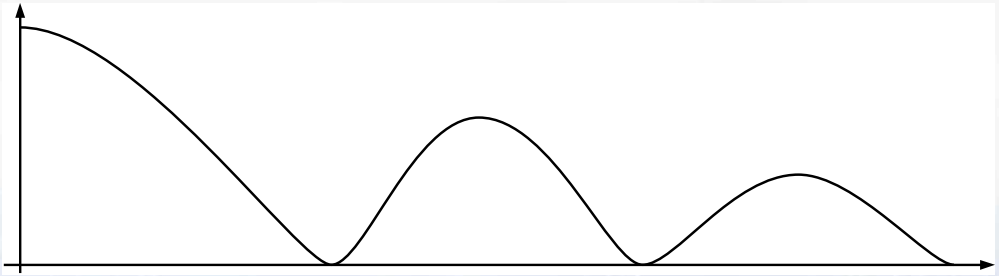
D/A conversion, cont'd

The output is a pulse-amplitude modulated signal (PAM)

$$A_{out}(t) = \sum a(nT) \cdot p(t - nT)$$

$$A_{OUT}(j\omega) = A\left(e^{j\omega T}\right) \cdot P(j\omega)$$

Commonly zero-order hold, since ideal reconstruction is impossible. In frequency domain output is sinc-weighted:



A reconstruction filter is needed to compensate!

D/A converter architectures

Current-steering

Outputs summed by weighted current sources.

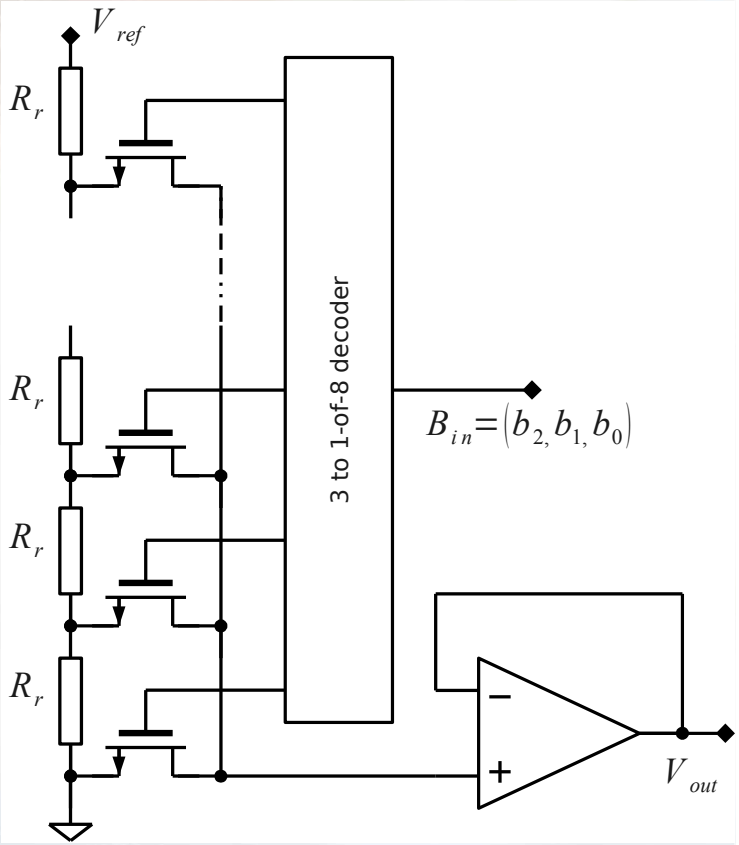
Resistor-string

Select one tap out of many and buffer

R-2R

Utilizes current dividers

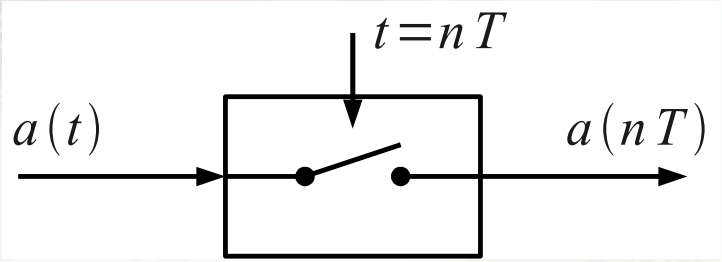
And many more



A/D conversion

A/D conversion is essentially a sampling process

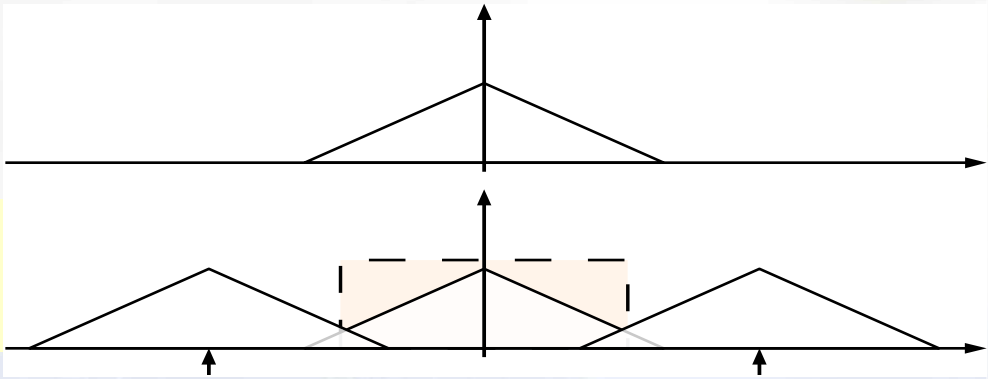
$$a(nT) = a(t)\big|_{t=nT}$$



Poission's summation formula

$$A\left(e^{j\omega T}\right) = \sum A\left(j(\omega - 2\pi k)\cdot T\right)$$

Spectrum might repeat and overlap itself!



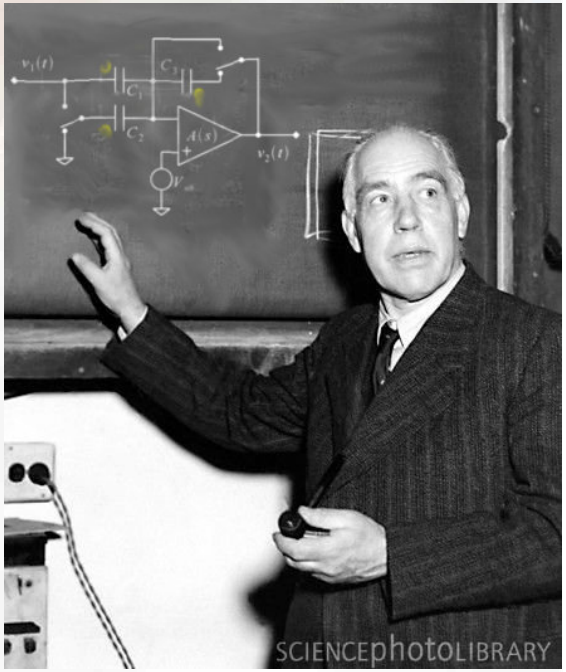
A/D conversion, cont'd

To avoid folding:

meet the sampling theorem (theoretically minimizes error)

use an anti-aliasing filter (practically minimizes error)

Practically, an amount of oversampling is required to meet the tough filter requirements



A/D converter architectures

The input is mapped on a digital code $D(nT)=\sum_{k=0}^{N-1} w_k(nT)\cdot 2^k$

Types

Flash: A set of comparators compare the input with reference levels

Sub-ranging: Use a coarse stage cascaded with a fine stage.

Pipelined: A set of sub-ranging ADCs

Successive approximation: One sub-ranging ADCs rather than a pipeline.

Converter trade-offs, speed vs resolution

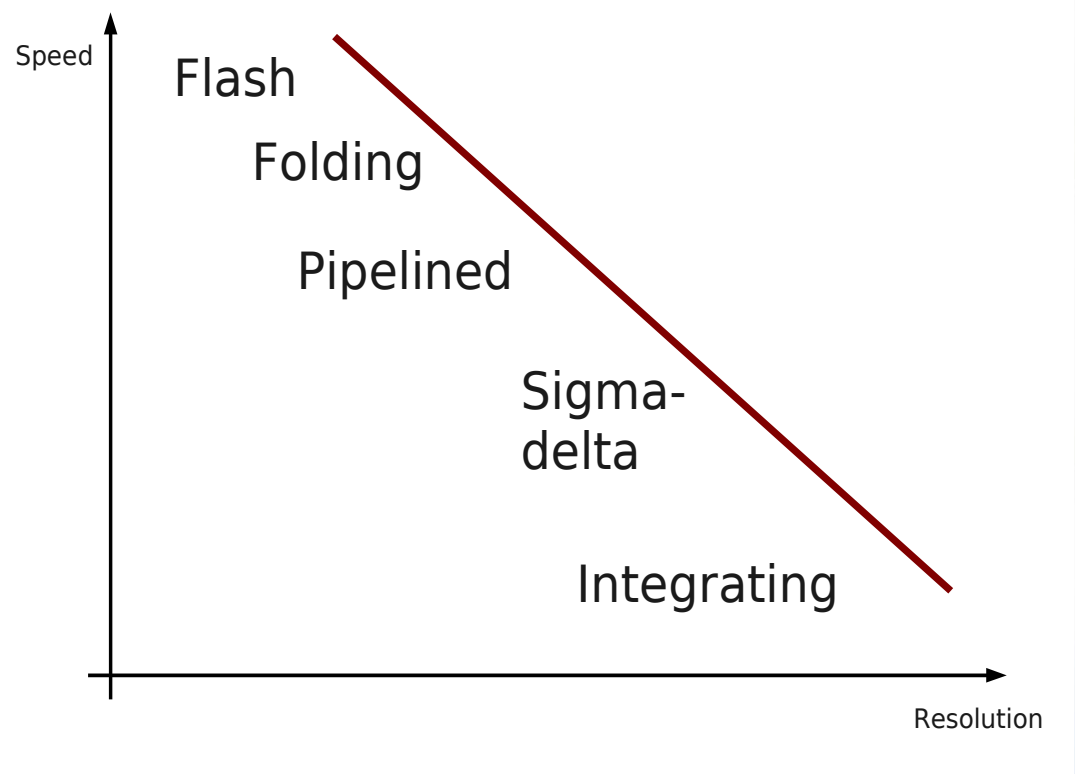
A common figure-of-merit:

$$\mathrm{FOM} = \frac{4kT \cdot f_{bw} \cdot \mathrm{DR}}{P}$$

Some conclusions from this formula

High-speed converters cost power

High-resolution converters cost area

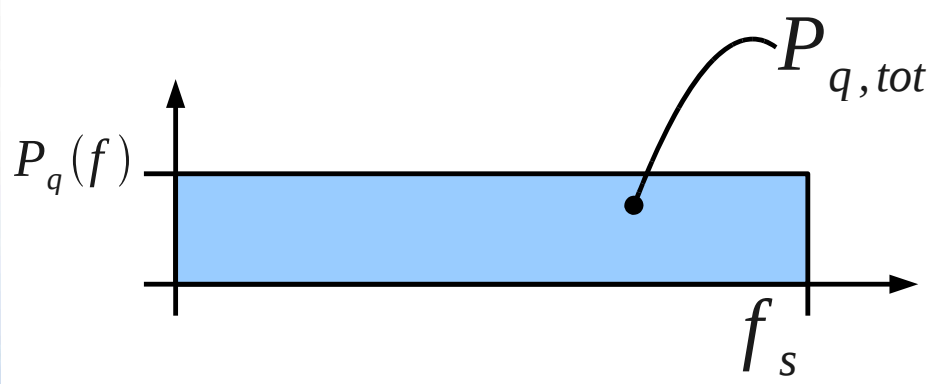


Quantization noise revisited 1

Assume signal-independent (not true for low number of bits)

Assume white noise, uniformly in $\left\{-\frac{\Delta}{2}, \frac{\Delta}{2}\right\}$**, with** $\Delta = \frac{V_{ref}}{2^N}$

Noise power spectral density (PSD)



Quantization noise revisited 2 (quiz ...)

Noise power given by the sigma: $P_{q,tot} = \sigma^2 = \Delta^2/12$

Signal-to-quantization-noise ratio: $\mathrm{SQNR} = \frac{P_{avg}}{P_{q,tot}} = \frac{P_{pk}}{P_{q,tot} \cdot \mathrm{PAR}}$

With values inserted $\mathrm{SQNR} = \frac{V_{ref}^2/4}{\frac{1}{12} \cdot \left(\frac{V_{ref}}{2^N}\right)^2 \cdot \mathrm{PAR}} = \frac{3 \cdot 2^{2N}}{\mathrm{PAR}}$

In logarithmic scale

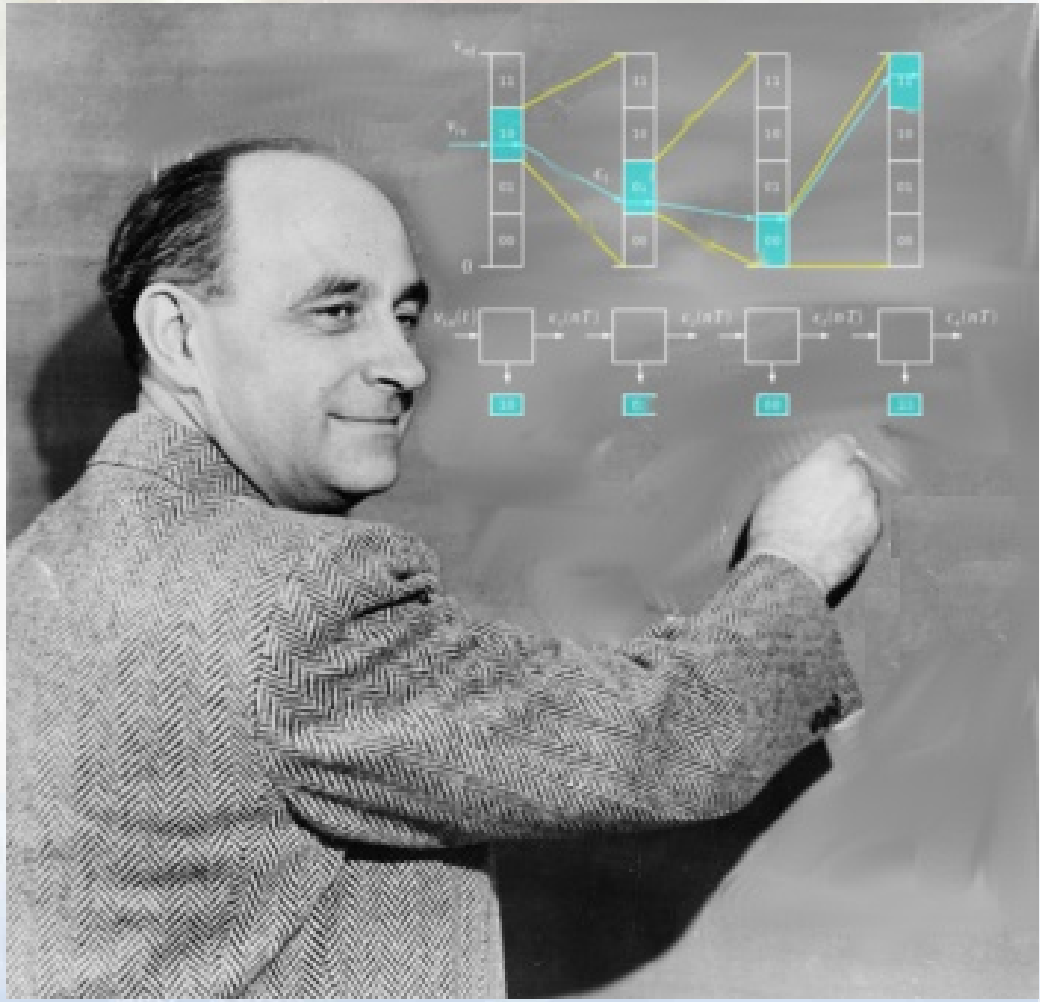
$$\mathrm{SQNR} \approx 6.02 \cdot N + 4.77 - \mathrm{PAR} = 6.02 \cdot N + 1.76.$$

Oversampling 1

Assume we have headroom to increase the sample frequency

Apply filtering to remove the excessive noise

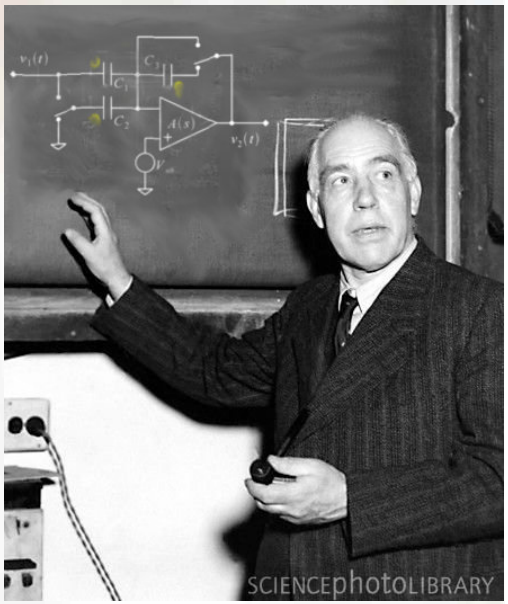
We can effectively increase the performance! Or ... ?



Oversampling converters

Noise power over the entire Nyquist range

$$\mathrm{SQNR} = 6.02 \cdot N + 1.76 \text{ [dB]}$$



Assume oversampling:

$$\mathrm{SQNR} = 6.02 \cdot N + 1.76 + 10 \cdot \log_{10} \frac{f_s}{2 \cdot f_{bw}}$$

where the oversampling ratio is $\mathrm{OSR} = \dfrac{f_s}{2 \cdot f_{bw}}$

"For each doubling of the sample frequency, we gain 3 dB"

Oversampling converters

Assume we take a lower order converter to start with

$$\mathrm{ENOB}=\frac{\mathrm{SQNR}-1.76}{6.02}=N+\frac{10\cdot\log_{10}\mathrm{OSR}}{6.02}$$

A 16-bit resolution can be obtained using a 12-bit converter if we oversample 256 times.

For some applications not an impossible scenario

A 16-bit resolution can be obtained using a 1-bit converter if we oversample 1073741824 times.

1 Hz would require 1 GHz of sampling frequency!

Attacking the filtering problem

Ideal reconstruction and sampling requires ideal filters

Increase your frequency range

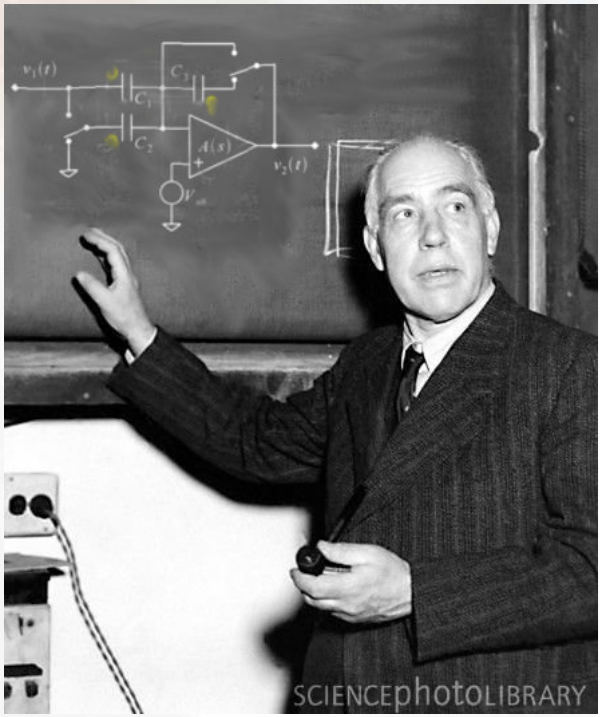
DAC: Interpolation and upsampling

ADC: Decimation and downsampling

Drawbacks

Higher power consumption

More difficult to design



Oversampling converters, cont'd

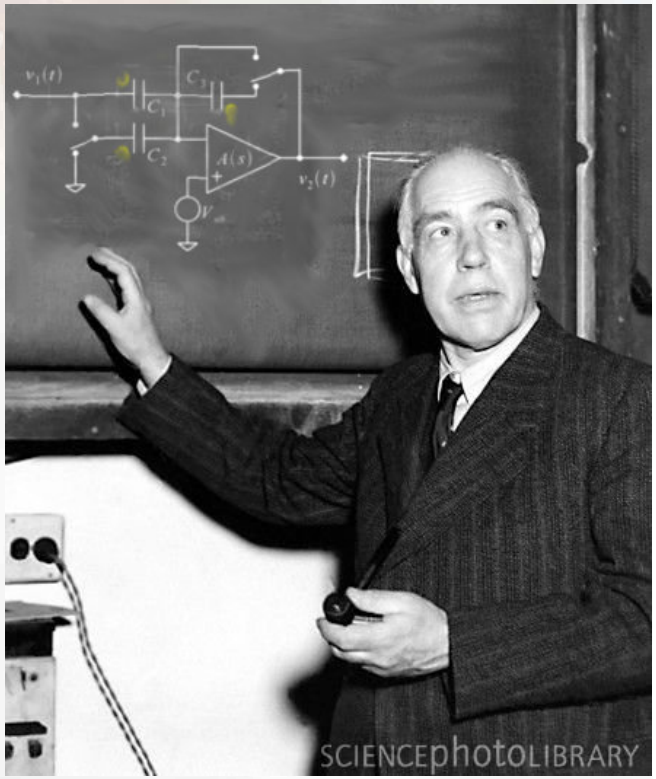
We introduce another converter, and increase frequency - why not more?

Create a converter that can also shape the new added noise

This is done by sigma-delta modulation

High-pass filters the added noise

All-pass filters the signal



Designing a sigma-delta modulator is a filtering problem

Notice that a DAC can never increase the number of bits!

Sigma-delta converters, cont'd

$$Y = Q + A \cdot \underbrace{\left(X - B \cdot Y \right)}_{\epsilon} \Rightarrow Y = \frac{Q + A \cdot X}{1 + A \cdot B}$$

Noise and signal transfer functions: $\mathrm{NTF} = \frac{1}{1 + A \cdot B}$, $\mathrm{STF} = \frac{A}{1 + A \cdot B}$

Example, A is integrator and B is unity: $\mathrm{NTF} = 1 - z^{-1}$, $\mathrm{STF} = z^{-1}$

Order of the filters and oversampling determines the SQNR:

$$\mathrm{SQNR} = 6.02 \cdot N + 1.76 + 10 \cdot (2 \cdot L + 1) \cdot \log_{10} \mathrm{OSR} - 10 \cdot \log_{10} \frac{\pi^{2L}}{2L + 1}$$

Sigma-delta converters, cont'd

1st-order modulator. 16 bits can be obtained using:

12-bit converter if we oversample 16 times
1-bit converter if we oversample 1522 times

Second-order modulator. 16-bit resolution ...

12-bit converter if we oversample 6 times.
1-bit converter if we oversample 116 times.

Third-order modulator. 16-bit resolution ...

12-bit converter if we oversample 5 times.
1-bit converter if we oversample 40 times

Sigma-delta, the audio example

HIFI

16 bits, i.e., 100 dB

Signal bandwidth

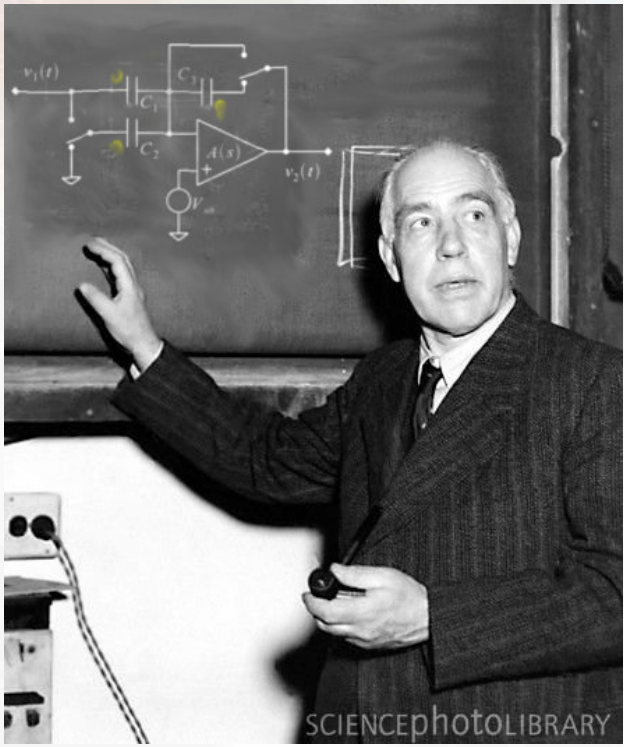
22 kHz

Choose few bits in quantizer

Choose minimum possible order

Choose minimum possible sample frequency

What configurations are possible?



Sigma-delta, the audio example

$$\mathrm{SQNR} = 6.02 \cdot N + 1.76 + 10 \cdot (2 \cdot L + 1) \cdot \log_{10} \mathrm{OSR} - 10 \cdot \log_{10} \frac{\pi^{2L}}{2L+1}$$

gives us

```
>> antikAudioSigmaDelta
SNR = 100.2442 dB, L = 2, M = 1, OSR = 128 fs = 5.632 MHz.      ******
SNR = 115.2957 dB, L = 2, M = 1, OSR = 256 fs = 11.264 MHz.
SNR = 106.2642 dB, L = 2, M = 2, OSR = 128 fs = 5.632 MHz.
SNR = 112.2842 dB, L = 2, M = 3, OSR = 128 fs = 5.632 MHz.
SNR = 103.2527 dB, L = 2, M = 4, OSR = 64 fs = 2.816 MHz.
SNR = 112.8346 dB, L = 3, M = 1, OSR = 64 fs = 2.816 MHz.
SNR = 103.8025 dB, L = 3, M = 3, OSR = 32 fs = 1.408 MHz.
SNR = 109.8225 dB, L = 3, M = 4, OSR = 32 fs = 1.408 MHz.
```

Föreläsning 7, PCB vs Si

Basic components and structures of PCBs
Transmission lines

LiU EXPANDING REALITY

Vad gjorde vi förra gången?

Noise

Thermal noise, an operational amplifier example

Flicker noise (1/f-noise)

Noise brickwall bandwidth: $\frac{p_1}{4}$

Distortion (pushed out to a lesson)

What sets the (non)linearity in our CMOS devices?

Vad kommer vi göra idag?

PCB vs silicon

What are the differences when scaling up the geometries?

Surface-mounted components

PCB specifics

Transmission lines

Termination techniques

Printed Circuit Board (PCB)

Layer stack

Up to 30 layers and more (the more, the more expensive)
Number of layers reduces due to the higher SOC integration, i.e., less need for interconnects. (Nvidia uses 10 layers or so).

Material

Al, Cu, 10 um thick, 60 um wide (example values!)

Generically

Larger, cm-scale

Limited options for selecting sizes, driving capability, etc.

Kisel

Layer stack

Up to some 10,12 layers
Number of layers increases due to higher integration.

Material

Aluminium, koppar, 300 nm thick, 200 nm wide (exempel)

Generically

Smaller, 25x25 mm -> 3.000.000.000 transistors (!!!)
“Any” option for selecting sizes, driving capability, etc.

Transmission line effects become more and more important!

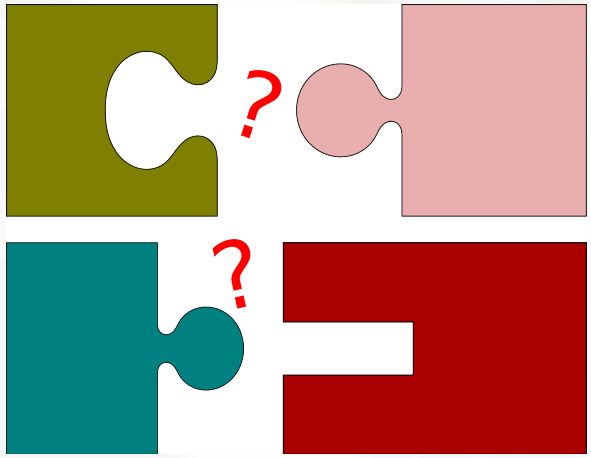
PCB vs. Silicon

Different nomenclature

Different tools and designers

Different ways to verify and fabricate

Heat, mechanical stress, etc., for example



... but essentially doing the same thing

Due to IP development (soft and hard subcells bought off-the-shelf), the assembly of the chip resembles PCB design.

More of an interconnect problem!

Surface-mount technology (SMx)

Old days

Hole through the entire PCB stack, effectively creating a large keep out in all layers.

Current trend

Smaller and smaller components (0.4 x 0.2 mm, “0402”). The smaller they get, the less power they tolerate, the smaller capacitors, inductors (< mH), etc.

A 0.4x0.2 resistor is rated for some 30 mW, **1 kOhm ~> 6 mA.**

Capacitor can be found in the **uF range.**

Implications of “size”

Large size implies physical components, wires, etc. behave as distributed components and not lumped (one “point”)

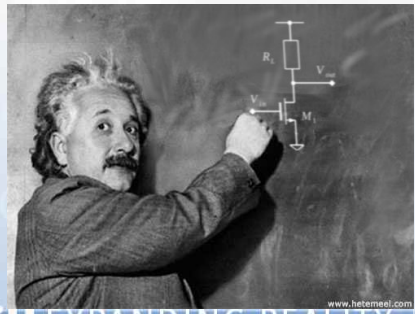
Distributed vs Lumped

t_r, t_f are the rise, fall times of a “digital” signal

t_d is the delay time through a wire, i.e., $t_d = \frac{l}{v} = \frac{l}{c/\sqrt{\epsilon_r}}$

Lumped elements: $t_r > 6 \cdot t_d$ **and** $t_f > 6 \cdot t_d$

Distributed elements: $t_r < 2.5 \cdot t_d$



Implications of “size”, cont'd

Notice!

Rise/fall time! Not only the frequency of the signal as such!

What about sinusoids?

“Mathematically”: $$l < 0.1 \cdot \lambda = 0.1 \cdot \frac{v}{f} = 0.1 \cdot \frac{c/\sqrt{\epsilon_r}}{f}$$

Practically: $$l < 0.01 \cdot \lambda = 0.01 \cdot \frac{v}{f} = 0.01 \cdot \frac{c/\sqrt{\epsilon_r}}{f}$$

At 2-GHz, the length must be > **1 cm/1 mm (!)** to be lumped!

More implications

Cross-talk

Wires will run a “long” distance next to each other and be sensitive to considerable mutual inductance.

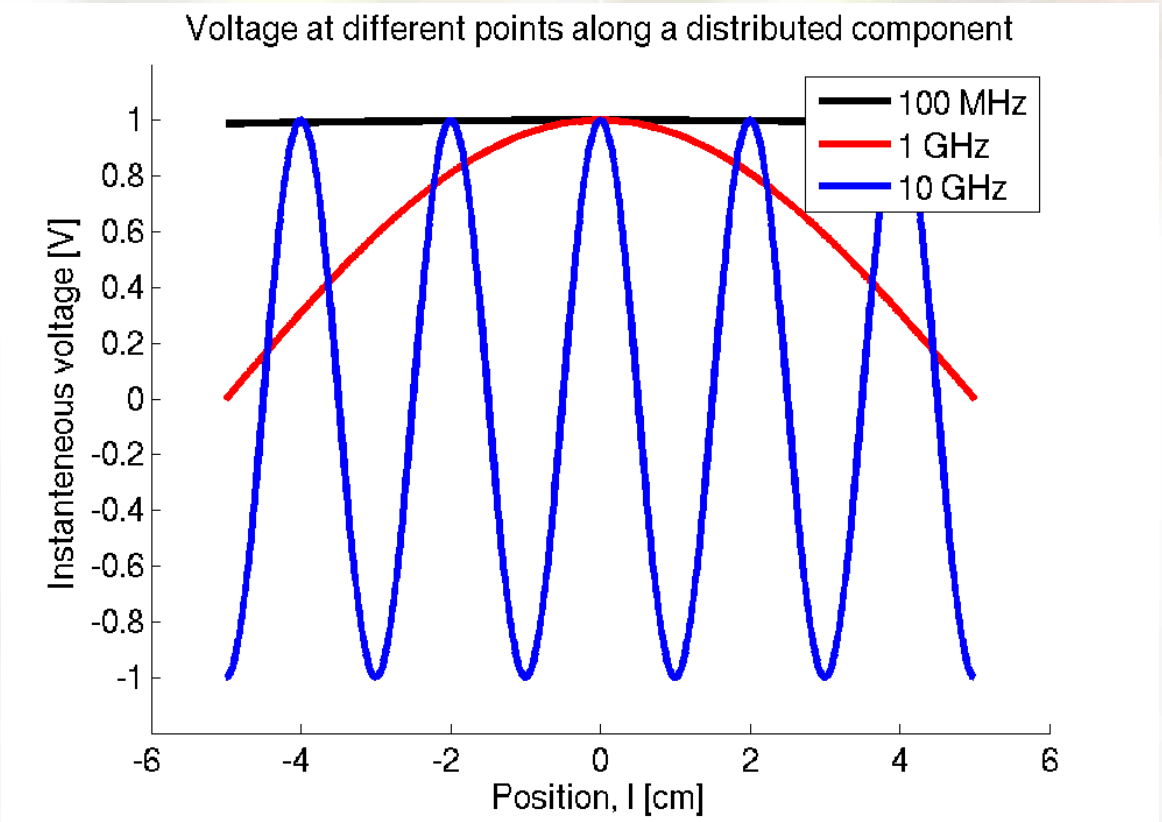
Return paths

With every voltage (current) in one direction, there has to be a return current. That return path could be different compared to the wire. (The return current takes path of least inductance).

Ringing and reflections

Due to the long wires, additional inductance, return paths, many more second-order effects are more visible

Implications of “size”, cont'd



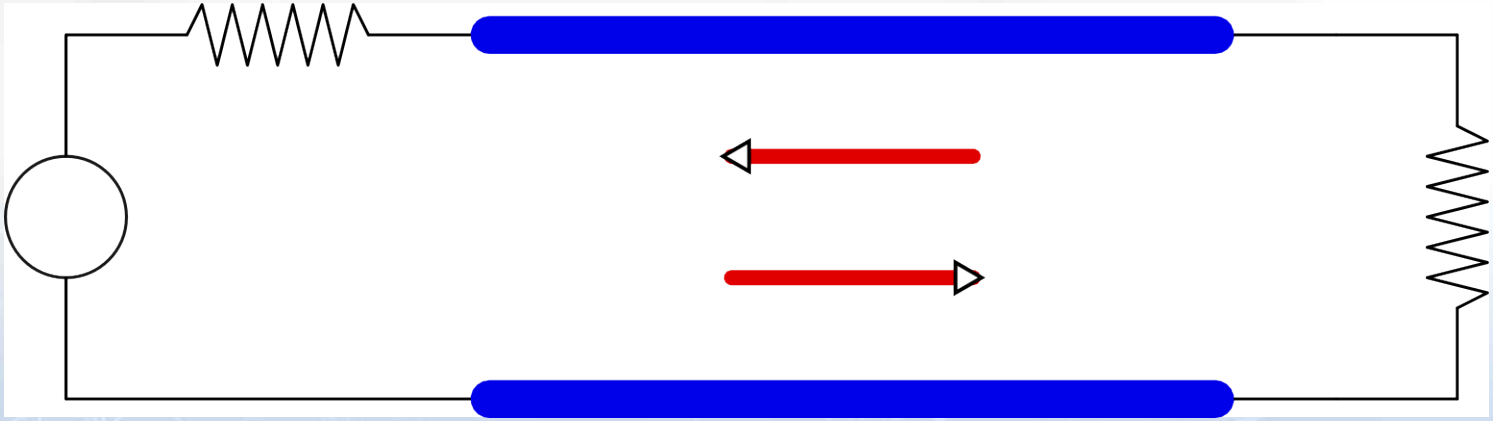
Cross-section must also be smaller than the wavelength (otherwise we get more prominent 3D-effects)

Transmission lines

Traveling wave

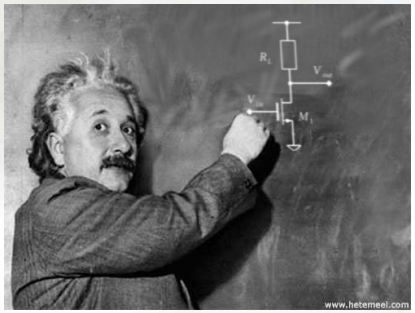
Consider the previous figure: the signal carrier (voltage, current, etc.) will travel as a wave over a surface.

This also holds for a pulsed waveform (i.e., not only the transient sinusoid). If we inject a pulse in one end, it will literally travel from one end to the other (and then?)



Transmission lines, cont'd

The Telegrapher's equations



$$\frac{d^2V(x)}{dx^2} = -(R + j\omega L)\cdot\frac{dI(x)}{dx} \text{ and } \frac{dI(x)}{dx} = -(G + j\omega C)\cdot V(x),$$

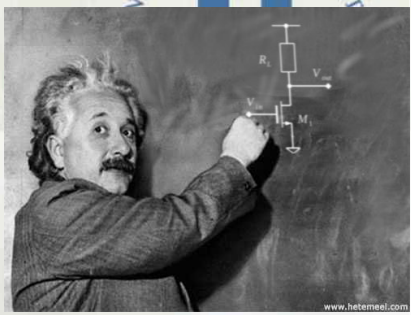
$$\frac{d^2V(x)}{dx^2} = \gamma^2\cdot V(x),\ \gamma^2 = (R + j\omega L)\cdot(G + j\omega C)$$

$$V(x) = V_{0p}\cdot e^{-\gamma x} + V_{0n}\cdot e^{\gamma x} \text{ and } I(x) = I_{0p}\cdot e^{-\gamma x} + I_{0n}\cdot e^{\gamma x}$$

R is the sheet resistance, G is the dielectric loss,

L and C are the inductance and capacitance.

Transmission lines, cont'd



Boundary conditions

$V_{0p}, V_{0n}, I_{0p}, I_{0n}$ determined by (e.g.) boundaries:

$V(0)=V_{0p}+V_{0n}$ and $I(0)=I_{0p}+I_{0n}$.

The characteristic impedance

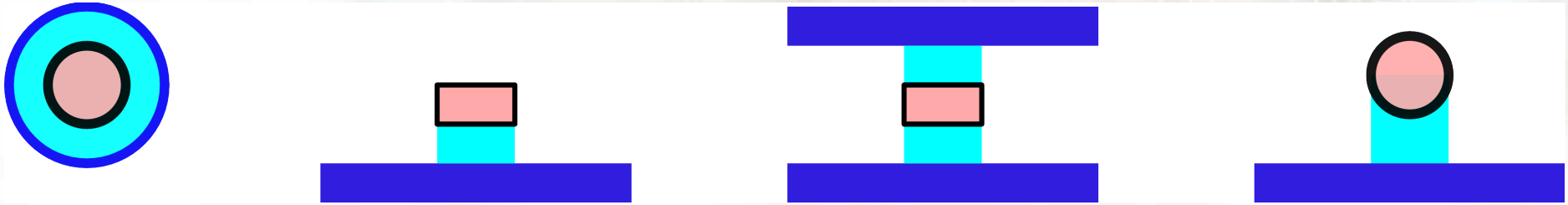
$$Z_0=\sqrt{\frac{R+j\omega L}{G+j\omega C}}$$ (independent on the wire length!)

$Z_0 \approx \sqrt{L/C}$ (lossless, often assumed for short wire/tracks)

C, L given by permeability wire/shield, and inductance.

Examples of transmission lines

Examples



A transmission line is created in any environment.

The intersection of the wire(s) define the properties of the transmission line. (Still, the wire can be tapered, i.e., intersection changes with length).

The choice of width, dielectric, height, width, etc., enables the designer to adjust the characteristic impedance.

Effects of source and load impedance

Reflections

Due to the impedance levels, a wave will be dependent on the impedance it sees in every node.

Reflection coefficient

$$\Gamma(x) = \frac{Z(x) - Z_0}{Z(x) + Z_0}$$

At the boundaries

$$\Gamma(0) = \frac{Z_S - Z_0}{Z_S + Z_0}$$ (looking “left”)

$$\Gamma(l) = \frac{Z_T - Z_0}{Z_T + Z_0}$$ (looking “right”)

Effects of source and load impedance

Examples of “extreme” cases:

$Z_{T,S}=0$, short-circuit. $\Gamma=-1$. Full reflection, negative phase.

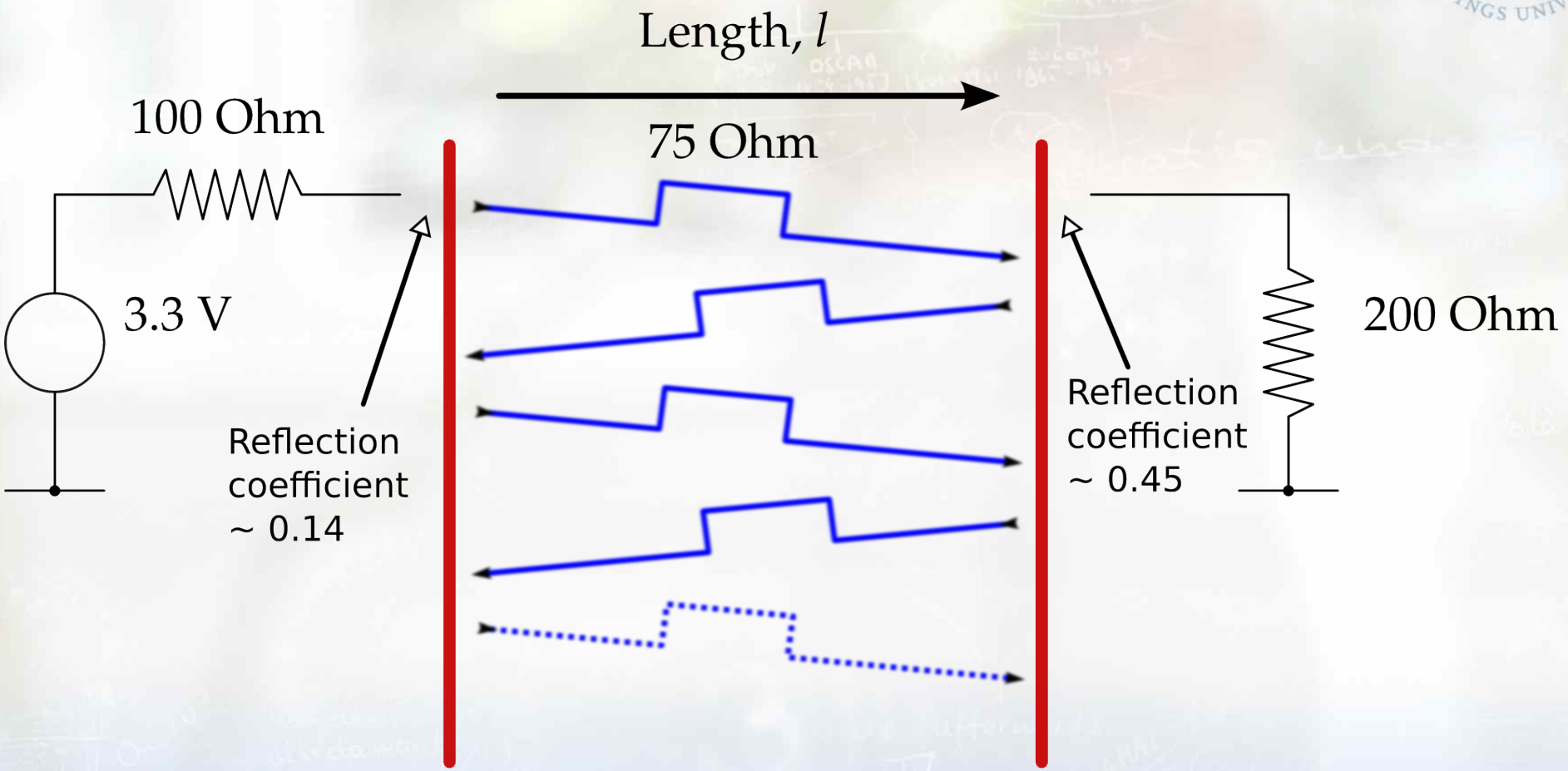
$Z_{T,S}=\infty$, open-circuit. $\Gamma=+1$. Full reflection with positive phase.

$Z_{T,S}=Z_0$, "perfect". $\Gamma=0$. Full absorption, no reflection.

Others

We can terminate with e.g. a capacitor too - a complex coefficient would give a phase shift. Normally, the driver is assumed to have very low impedance.

Reflection diagram



Reflection diagram, cont'd

First outgoing wave amplitude is: $V_{out} = 3.3 \cdot \frac{75}{75 + 100} \approx 1.41$

This wave arrives at load and is also reflected.

First returning wave amplitude is: $0.45 \cdot 1.41 \approx 0.64$.

We get at the load: $V_l = 1.41 + 0.64 \approx 2.06$

Wave goes back to source and is reflected: $0.14 \cdot 0.64 \approx 0.21$.

Reflection diagram, cont'd

Reflected at receiver: $0.45 \cdot 0.21 \approx 0.091$.

We get $V_l = 2.06 + (1 + 0.45) \cdot 0.091 \approx 2.19$

etc. until we end up at

$$V_l = 3.3 \cdot \frac{200}{200 + 100} = 2.2$$

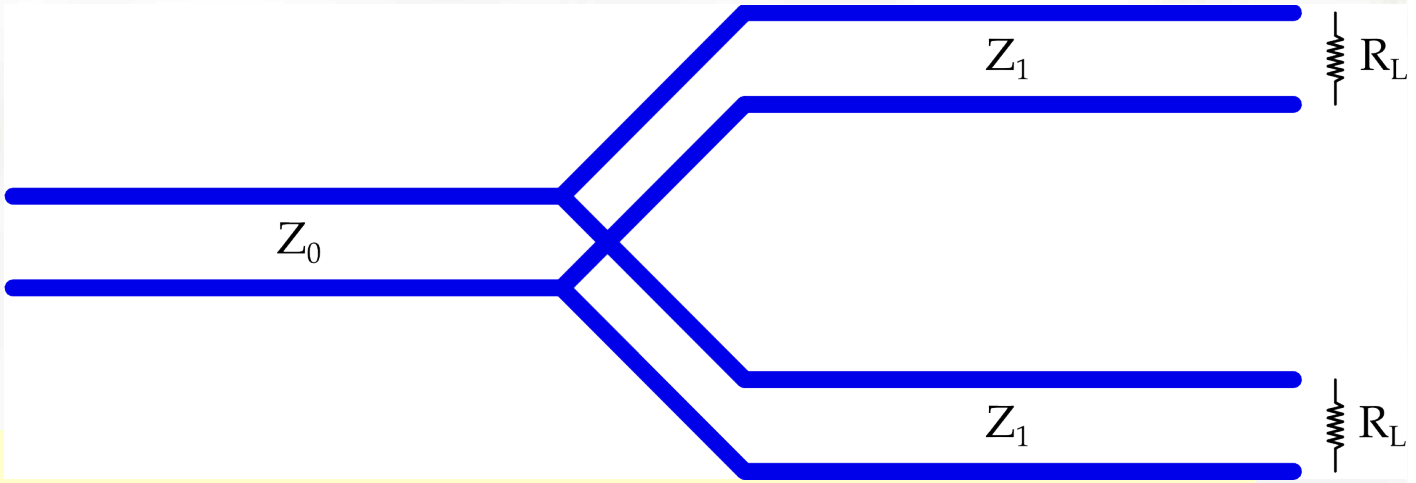
Delade (bifurcated) ledningar

$Z_0 = Z_1$ ger reflektion, oberoende av R_L.

Taper the impedance, $Z_1 = 2 \cdot Z_0$!

Terminera

$R_L = Z_1 = 2\,Z_0$



Impedanserna
måste vara anpassade vid brytpunkten.
Hur ser det ut med många grenar?

Oterminerade ledare (lasten)

Låg utimpedans (källa)

Vid lasten ackumuleras spänningen och blir högre än drivspänningen

Liknar ringning, dvs odämpat insvängning

Hög utimpedans (källa)

Små, inkrementella steg mot slutvärdet

Liknar dämpad insvängning

Serieterminering i källan (back-matching)

Can be used together with open-circuit receivers

Series resistor between driver output and transmission line

Cuts amplitude to 50% before "entering" transmission line

Full reflection at end, +1 due to open-circuit load. This will effectively form a full swing at the receiver (!)

Reflected wave?

Absorbed at the source due to the source termination

Driver output current goes to zero when reflected wave arrives

Källterminering, forts

Krav

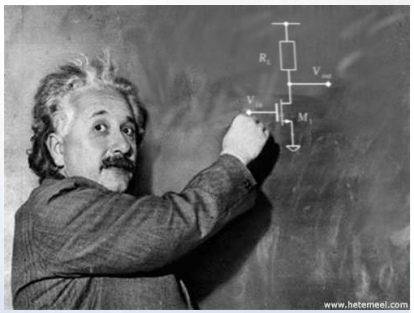
Cascaded internal and series resistance must equal Z_0!

How close must source termination be?

Stub (inductive!, e.g. bonding wires + PCB strips) between driver and termination will produce reflection.

Om man har två ledare?

Placera ett eller två termineringsmotstånd



Comparison end vs source termination

Source usually resistive (plus inductance), end usually capacitive

Mismatch between characteristic impedance and capacitive load generally worse than the series resistor mismatch

Usually less reflections traveling back and forth in source termination!

DC biasing of end termination

Termination resistor only to ground

Driver has to deliver a very high current when switching high.

Possible skew in duty cycle (faster pull down)

Termination resistor between ground and supply (Thevenin)

Select R_1 and R_2 such that $Z_0 = R_1 \| R_2$, i.e., $R_1 = \frac{R_2 \cdot Z_0}{R_2 - Z_0}$

Lower current for driver, but both when switching low and high

A DC current $I_{avg} = V_{DD} / R_1 + R_2$ will be "wasted"

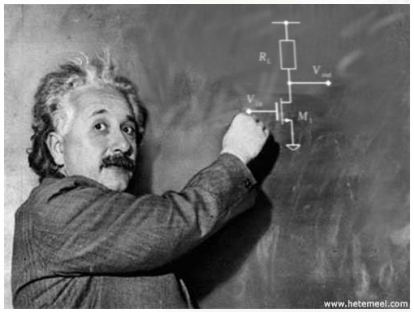
AC biasing of end termination

Använd en kondensator i serie med motståndet $(R = Z_0)$

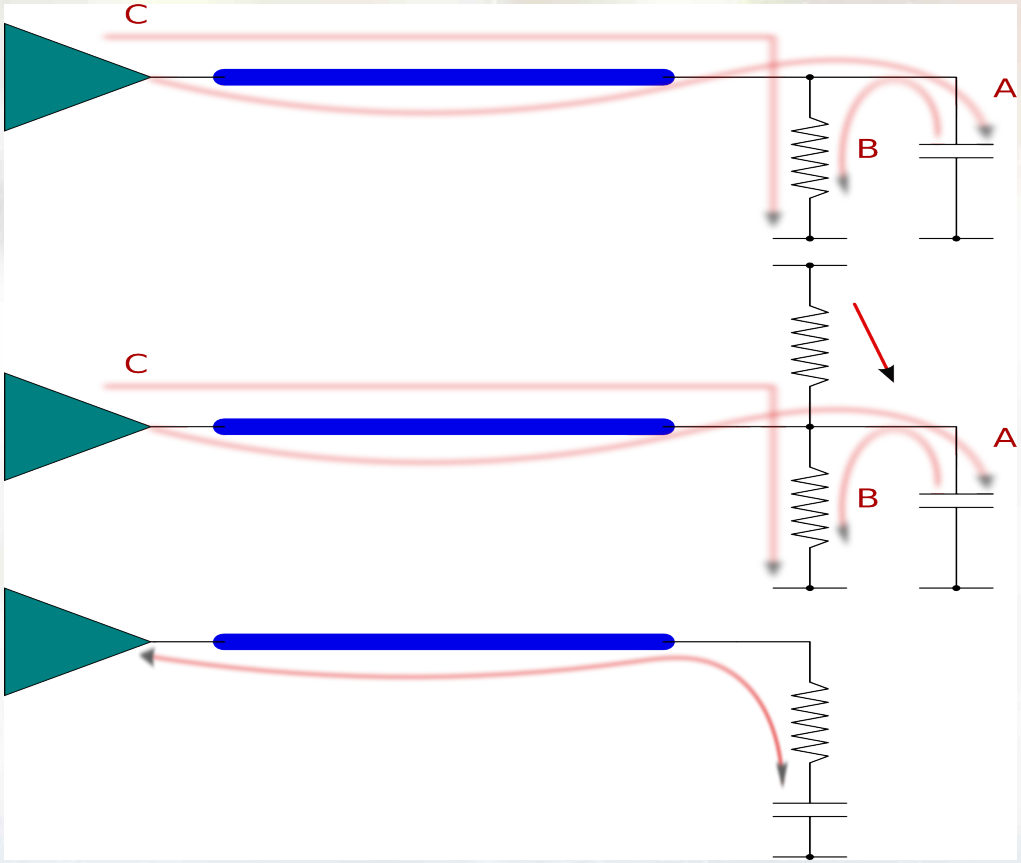
Wastes less current compared to the DC biasing scheme (no current consumed at "DC")

But - must have a DC balanced signal, i.e., 50-% duty cycle, i.e., suitable for a clock driver.

Restrictions on the capacitor



DC/AC biasing of end termination



Korta vågledare

Väldigt korta ledare

Till exempel ledaren från avkopplingskondensatorn till chip-matningen/jorden

Vias

Även en via kommer vara en kort ledare och ha en karakteristisk impedans.

Undvik vior på känsliga ledare!

Vad gjorde vi idag?

PCB vs kisel

Höga hastigheter och snabba flanker gör att vi måste betrakta vågledarteori

Vågledare

Terminering och andra egenskaper

Vad står på tur nästa gång?

Matningsfilter

Avkopplingskondensatorer

Frekvensgång på ett PCB

Föreläsning 8, Avkopplings-kondensatorer

Matningsnät, frekvensgång, med mera.

LiU EXPANDING REALITY

Vad gjorde vi förra gången?

Vågledare

Terminering

Vad ska vi göra idag?

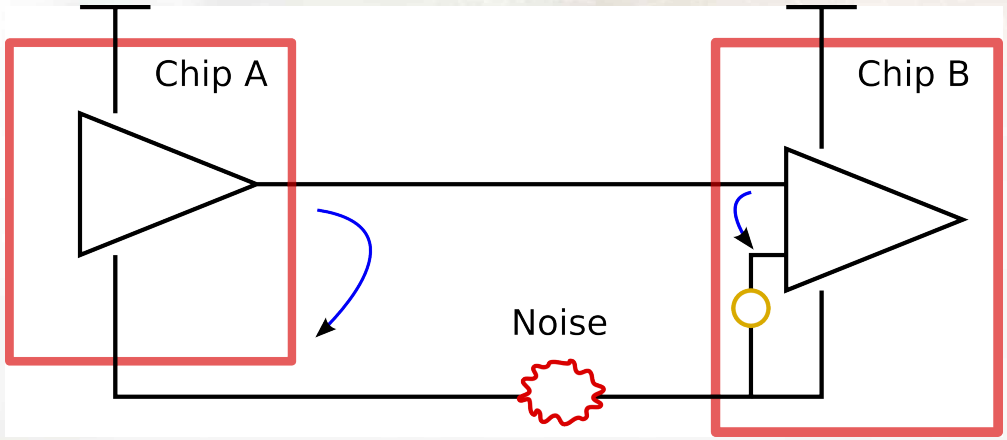
Avkopplingskondensatorer

Matningsnät

Hur ska man koppla av?

Betrakta ett PCB: matningsfilter

Receiver picks up noise on the ground (reference) wire



Noise sources

External humm (50, 60 Hz) and other interferers
Due to shared ground paths due to inductance in path
Differential signalling solves a lot (see next lecture)

The power rules

Three rules for power supplies/grounds

1) Use low-impedance ground connections between chips (gates).

2) The impedance between power pins on any two chips (gates) should be just as low as the impedance between ground pins.

3) There must be a low-impedance path between power and ground

The power rules, cont'd

These three rules can be satisfied if:

There is a good ground plane and there are bypass capacitors close to each chip/gate/component providing the low-impedance path.

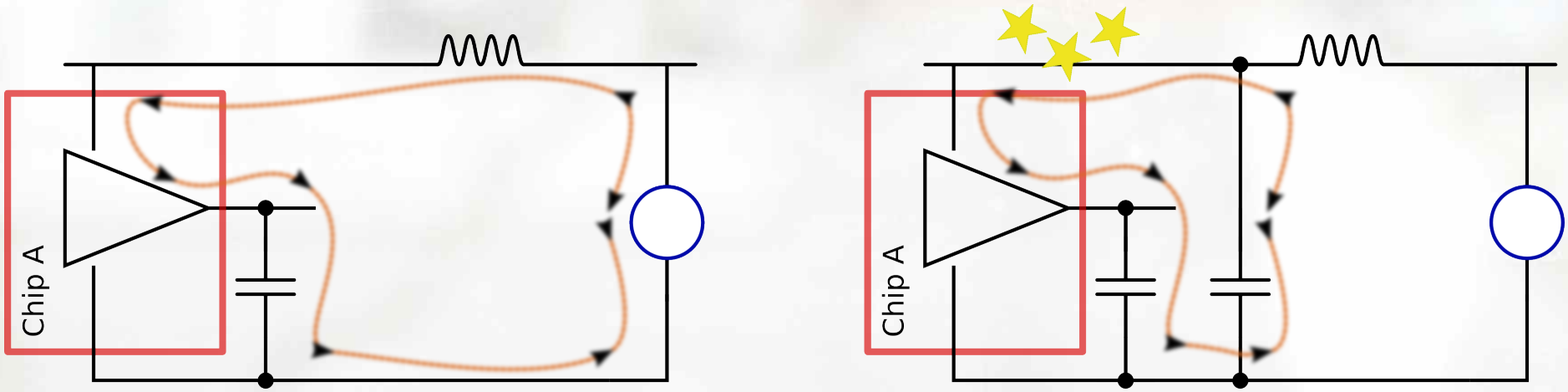
Then, the supply wiring can be “sloppy”.

(However, best to use a power supply plane too).

Om nu matningsledaren är "sloppy". Vad händer då?

Supply filters (bypass capacitors)

Connecting a bypass capacitor locally also reduces the effect of inductance in the supply wires.



Supply has low impedance at low frequencies (inductance)

Capacitor has low impedance at high frequencies

Exempel, avkopplingskondensator

Antag

Power inductance is L_P and that the max power drop ΔV

Chip switches N wires, each with a load of C_L during t_{rf}

Några förhållanden

$$\Delta I = N \cdot C_L \cdot \frac{V_{dd}}{t_{rf}},\ \Delta V = X_{max} \cdot \Delta I,\ X_{max} = 2\pi \cdot L_P \cdot f_x$$

Exempelvärden

$$V_{dd} = 1\,V,\ N = 16, C_L = 10\,pF,\ L_P = 100\,nH,\ \Delta V = 100\,mV,\ t_{rf} = 100\,ps$$

Exempel, avkopplingskondensator, forts

Kombinera och förenkla (antag Z = X - utsläckning)

$$C_x = \frac{1}{2\pi \cdot f_x \cdot Z_{max}} = \frac{1}{2\pi \cdot \frac{X_{max}}{2\pi L_P} Z_{max}} = \frac{L_P}{X_{max}^{\ 2}} = \frac{L_P}{\left(\frac{\Delta V}{\Delta I}\right)^2} = \frac{L_P}{\left(\frac{\Delta V}{N \cdot C_L \cdot \frac{V_{dd}}{t_{rf}}}\right)^2}$$

Kondensatorns reaktans kommer släcka ut effekten av spolen då

$$C_x = \frac{\left(N \cdot C_L \cdot V_{dd}\right)^2 \cdot L_P}{\left(\Delta V \cdot t_{rf}\right)^2}$$

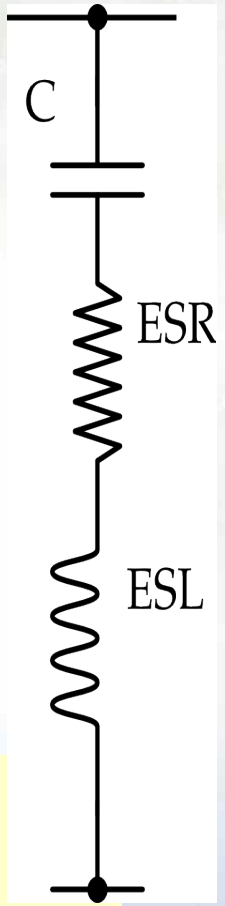
$$C_x \approx 37\,\mu F$$

Decoupling (bypass) capacitors

Parasitics

Lead/package/mounting inductance, L

Equivalent series parasitic resistance



Effective inductance

$$Z_C(\omega) = \sqrt{ESR^2 + \left(\omega L - \frac{1}{\omega C}\right)^2}$$

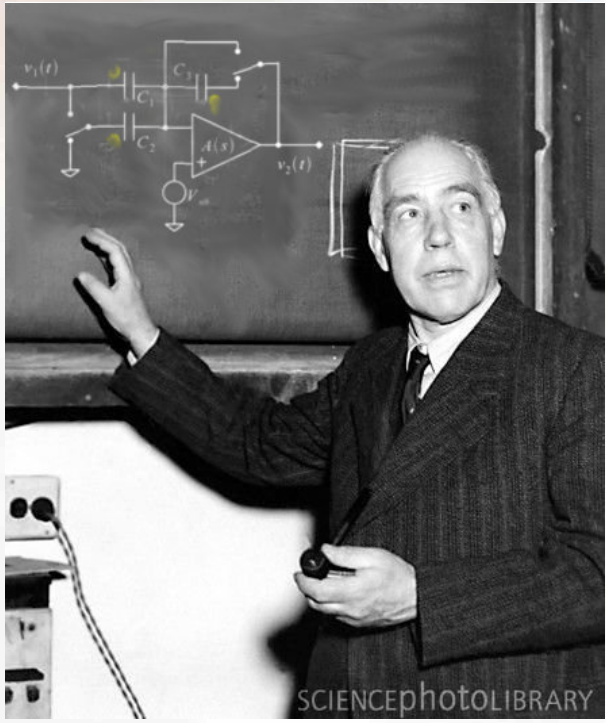
The L and C can give rise to resonance effects when connected in parallel!

Decoupling (bypass) capacitors

Requirements on the reactance/impedance

0.1 to 1 Ohm

Figure showing the impedance effects



1) Wiring inductance from supply

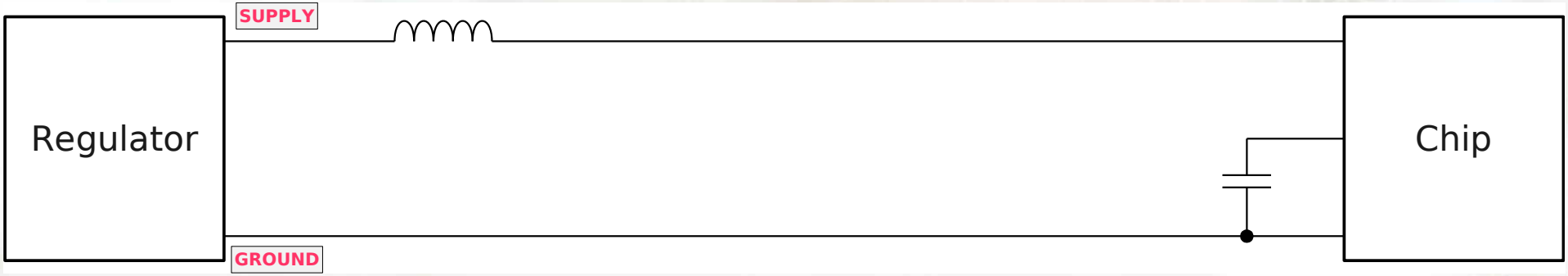
2) Decoupling capacitors

3) Decoupling capacitive bank

4) Power and ground plane

The power net impedance

Inductance of supply wire

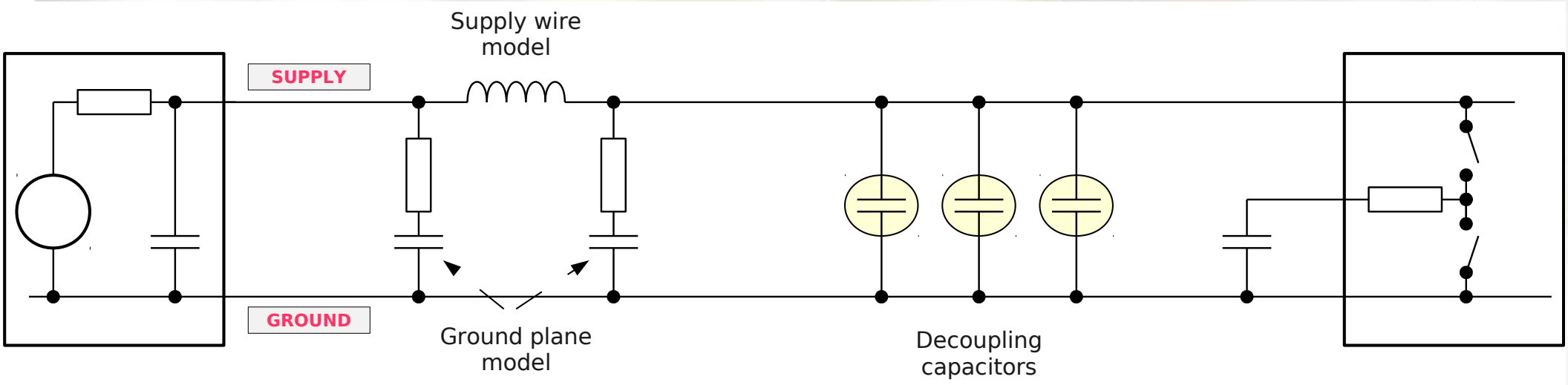


Current spikes through inductance cause voltage drops

Current spike generated due to switching of capacitor in load

Voltage generated by regulator/battery/voltage source

The power net impedance, cont'd

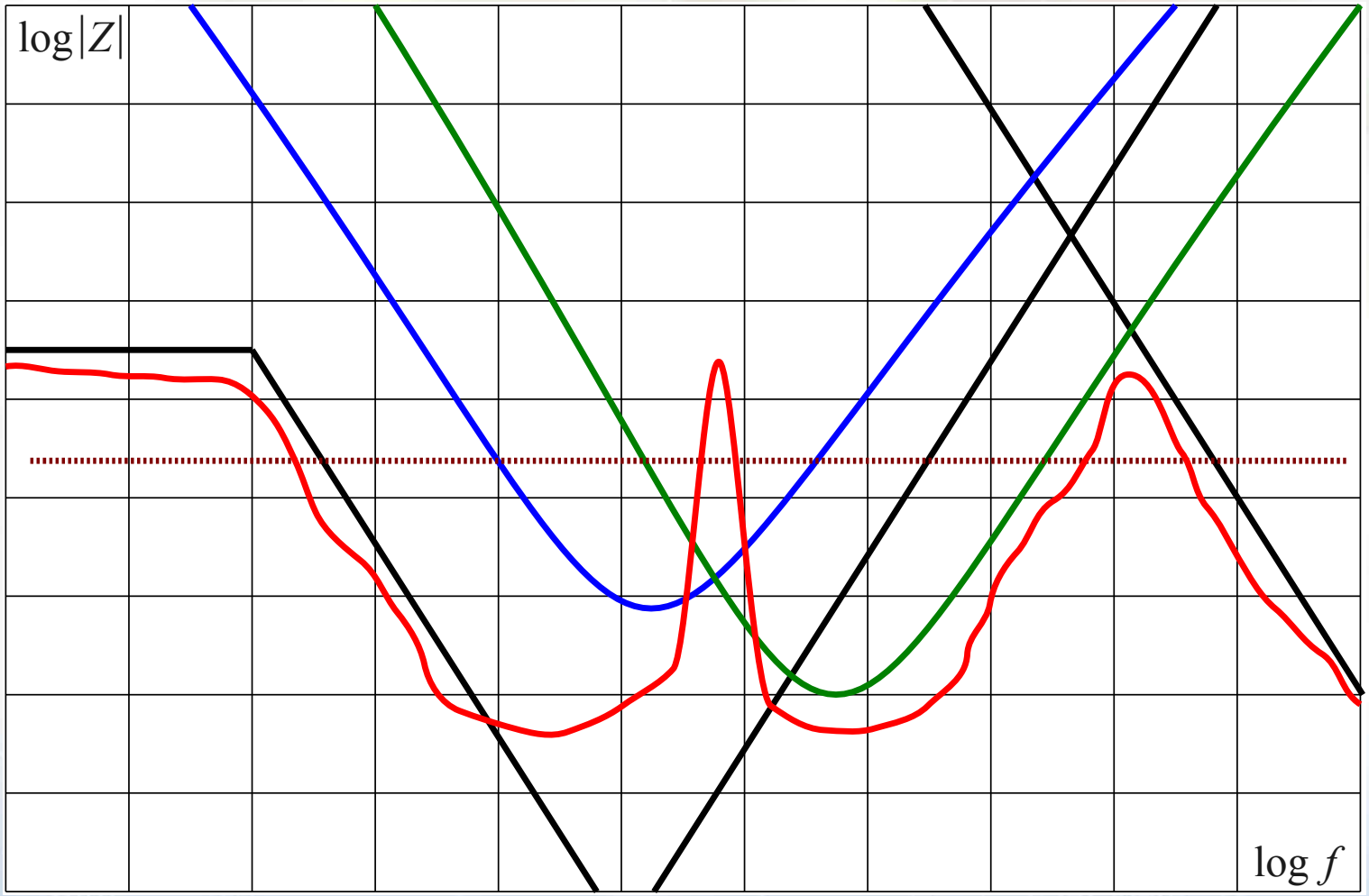


Investigating the supply in the supply node (at the receiver)

Regulator bandwidth
Ground plane (mainly capacitive)
Supply wire (mainly inductive)

Decoupling capacitors to further reduce impedance

Impedansgrafen



Hur ska man välja?

Så många som möjligt av samma storlek (helst små!)

Kostnad måste tas i beaktande.
Diskreta komponenter är dyra.

Hur mycket måste man undertrycka störningarna?

Specifikationsdrivet (inom vissa frekvenser, blah blah)

Använd stora jord och matningsplan

Laborationer!

Differentiella signaler

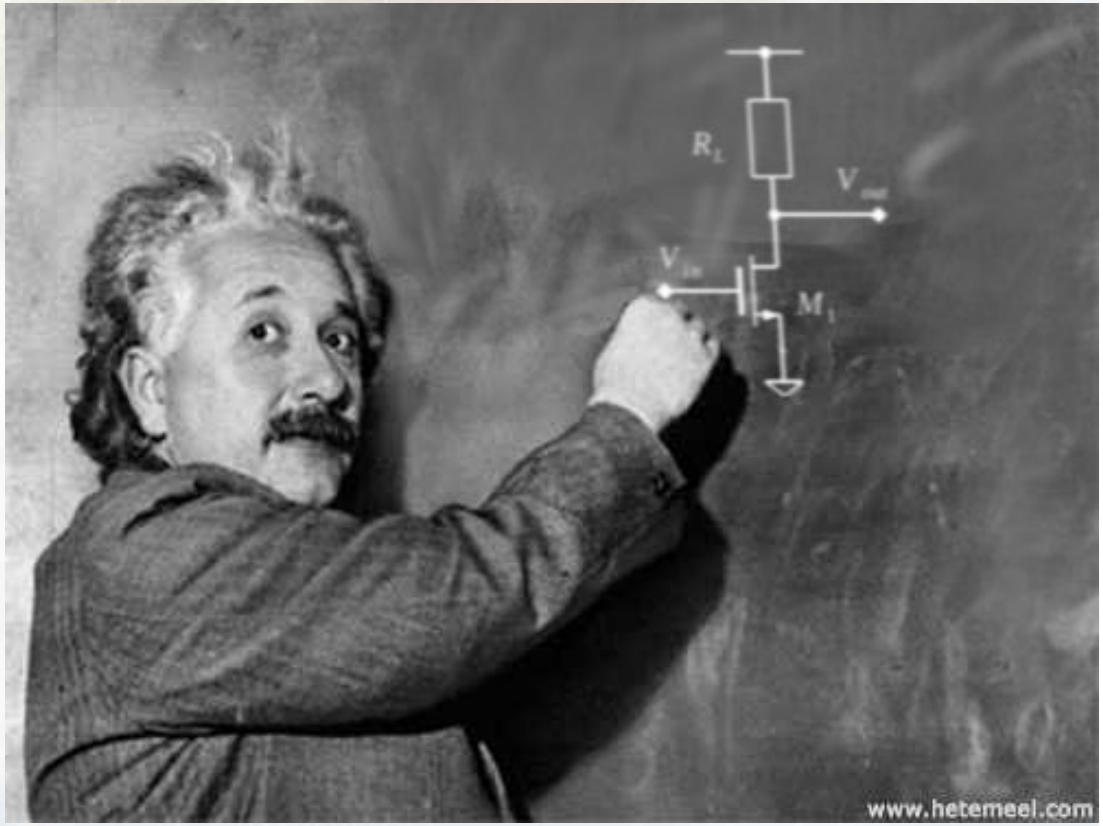
Differentiella signaler

$$\Delta V = V_p - V_n$$

Common-mode signal

$$\nabla V = \frac{V_p + V_n}{2}$$

Common-mode undertryck-ning



Differential signals, the matrix compiled

Compile the transfer functions into a handy matrix

$$\begin{bmatrix} \Delta V_{out} \\ \nabla V_{out} \end{bmatrix} = \begin{bmatrix} A_{df} & A_{df,cm} \\ A_{cm,df} & A_{cm} \end{bmatrix} \begin{bmatrix} \Delta V_{in} \\ \nabla V_{in} \end{bmatrix}$$

Common-mode rejection ratio

$$\mathrm{CMRR} = \frac{A_{df}}{A_{cm}}$$

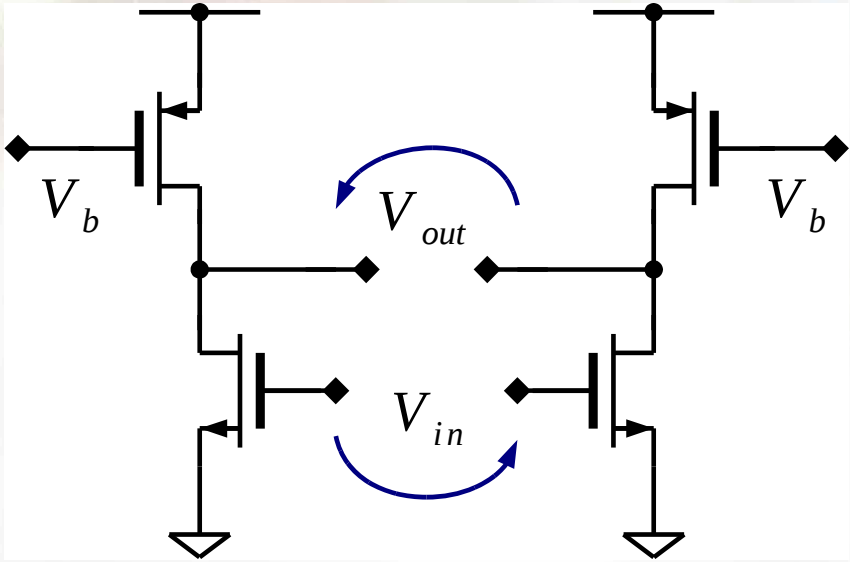
Design targets

Maximize differential gain, Minimize common-mode gain

Differential signals, two CS stages

Common-mode range (CMR)

Common-mode levels for which the transistors operate in saturation



What about rejection?

If there is no rejection, the voltage headroom might be severely affected.

Without rejection, no real use (except for slight gain in SNR)

Effectively there is no rejection in this configuration!
Some kind of "glue" is neeed.

Differential signals, cont'd

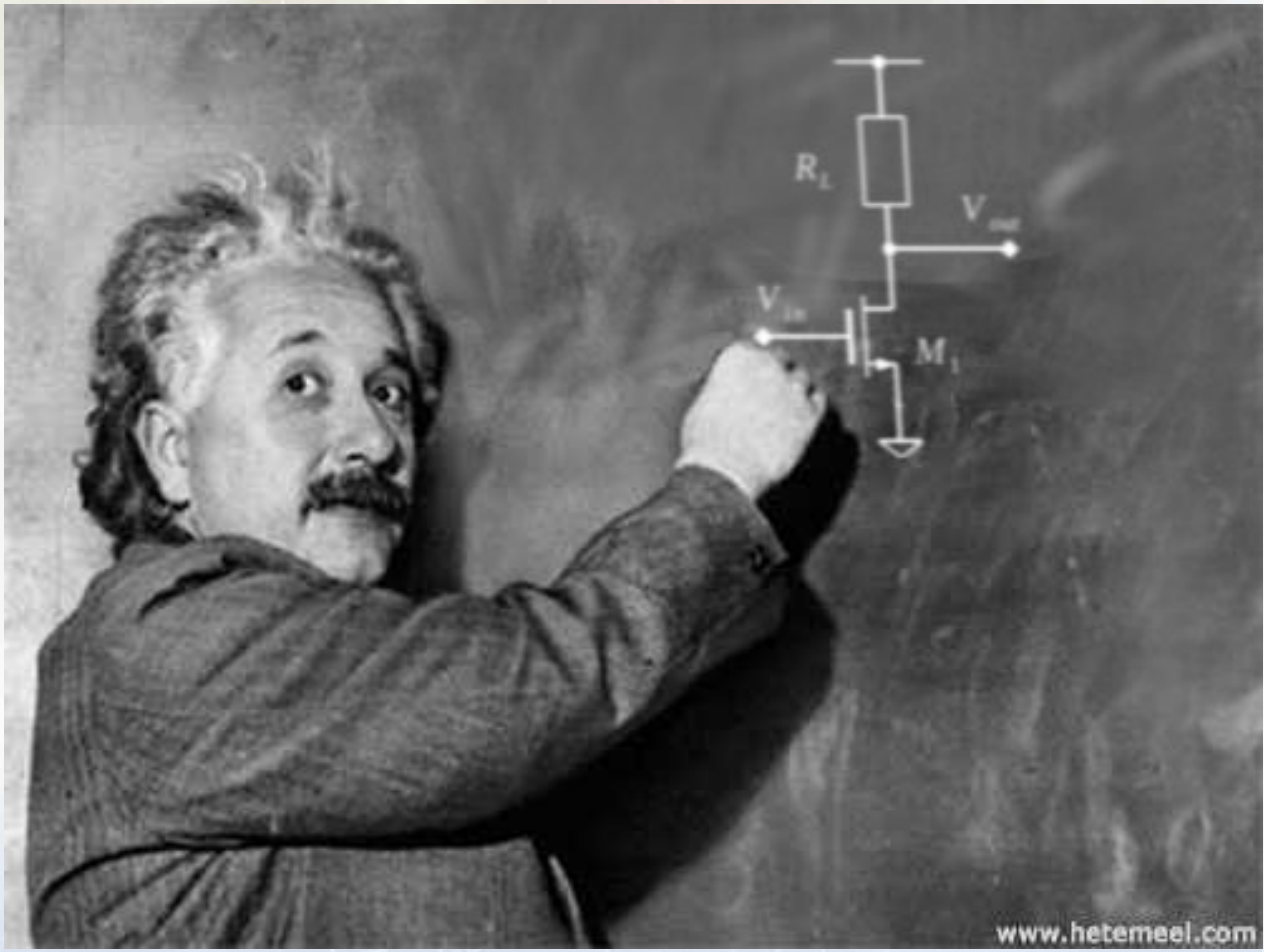
Two common-source stages in parallel

$$\mathrm{CMRR} = \frac{A_{df}}{A_{cm}}$$

The differential pair

Tail source

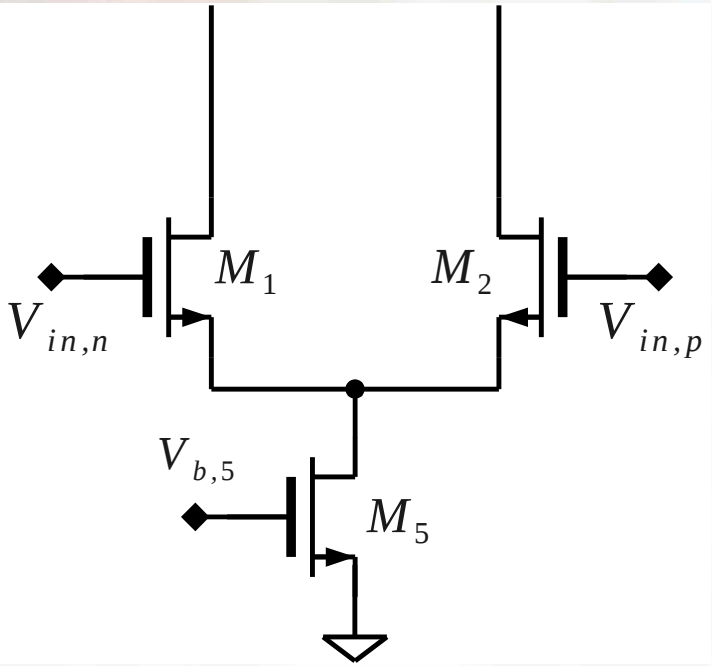
$$\mathrm{CMRR} = \infty$$



Differential signals, differential pair

Improved CMRR to cost of CMR

$\Delta I = 4\alpha \cdot V_{eff} \cdot \Delta V$ and $\nabla I = I_0/2$ (!)



Further on

$$I_0 = 2\alpha \cdot \left(V_{eff}^2 + \Delta V^2 \right)$$

combines into

$$\Delta I = 4\alpha \cdot \Delta V \cdot \sqrt{\frac{I_0}{2\alpha} - \Delta V^2} \quad (!)$$

$$\frac{d\Delta I}{d\Delta V} = 4\alpha \cdot \sqrt{\frac{I_0}{2}} = 4\alpha V_{eff} = \frac{2I_0}{V_{eff}}$$ and $$\frac{d\nabla I}{d\nabla V} = 0$$

Jordplan vs differentiella signaler

Minimizes the need for well-defined common reference

For example the ground

Improves the signal-to-noise ratio (by some 3 dB)

Single-ended signal power: $P_{s,s}=\frac{V_s^2}{2}$ and noise power: $P_{n,s}=V_n^2$

Differential signal power: $P_{s,d}=\frac{\left(V_s-\left(-V_s\right)\right)^2}{2}=2\cdot V_s^2=4\cdot P_{s,s}$ and

noise power $P_{n,d}=\left(V_{np}+V_{nn}\right)^2=V_{np}^2+V_{nn}^2=2\cdot P_{n,s}$

Vad gjorde vi idag?

Matningsnät

Avkopplingskondensatorer

Regulatorer

Kort översikt

Vad står på tur nästa gång?

Distribuera signaler

- Klockor
- Digital data

Timing and klockning

- Tidssynkronisering
- Mot PLL, DLL

Föreläsning 9, Timing, clocking

Differential signaling schemes
Timing and clocking

LiU EXPANDING REALITY

Vad gjorde vi förra gången?

Matningsfilter

Avkopplingskondensatorer

Matningsimpedansen

Differentiella signaler

Returströmmarna kryper under signalledarna i single-ended

Differentiella signaler undertrycker gemensamma störningar och låter returströmmen ta en kontrollerad väg tillbaka.

Vad kommer vi göra idag?

Signaldistribution

Olika signalleringsformat

Timing and clocking

Skew and clock tree structures

A first glance at the PLL and clocking scenarios between chips

Signalling

A set of different signalling standards between chips

CMOS, TTL, ECL, CML, LVDS

Can be in different flavours

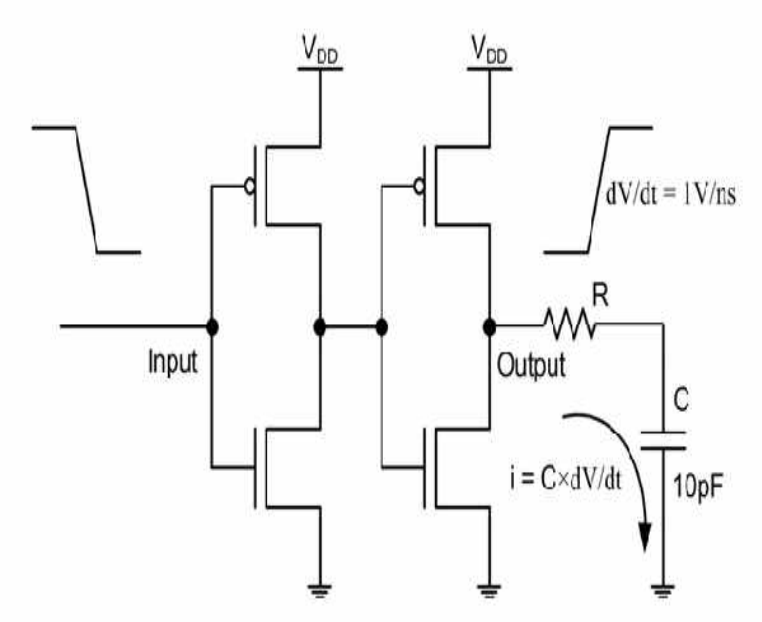
Swings, supply levels, current levels, etc.

Can have additional twists

Coding schemes

Some single-ended formats have differential modes.

CMOS (Complementary MOS)



Single-ended, CMOS

Voltage-driven and toggles between supply and ground.

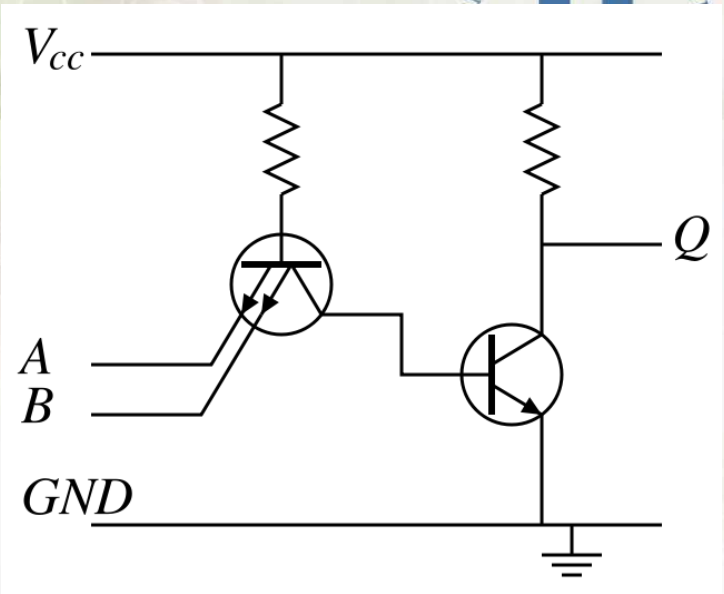
Maximum speed ~ 500 MHz

"Simple"

Power consumption is increasing with frequency and has a high impact on the chip IO ring (large switches and high dI/dt)

Infinite input impedance, Low output impedance

TTL (Transistor-transistor logic)



Single-ended, bipolar

Current-driven. "Current-sink logic", i.e., current pulls down. No current implies that receiver pulls-up "by itself". Toggles supply and ground.

Maximum speed ~ 200 MHz

"Simple"

High power consumption

Low input impedance, high/low output impedance.

ECL (Emitter-coupled logic)

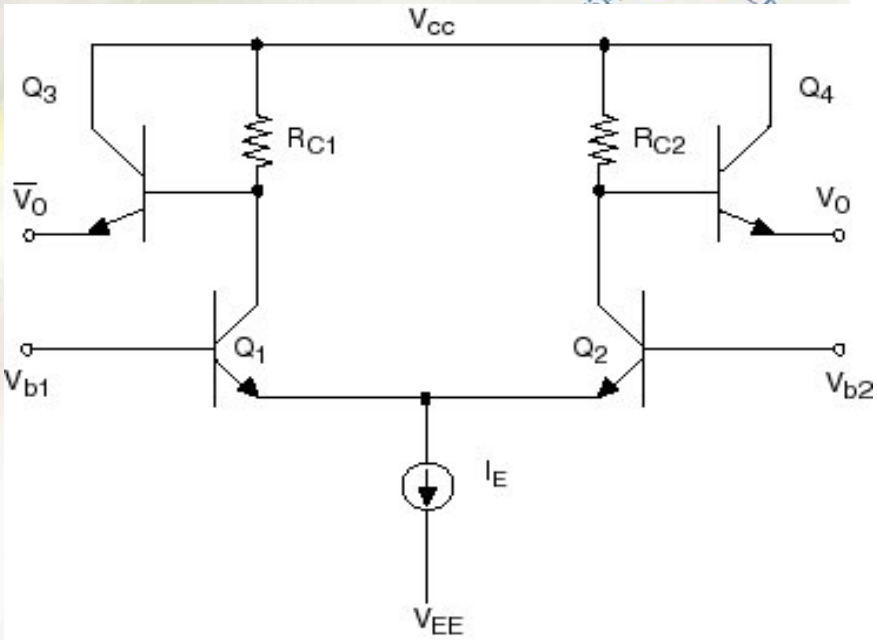


Figure 1 The Basic ECL Circuit

Single-ended, bipolar

Current-driven. Current pulls down. No current implies that receiver pulls-up "by itself".

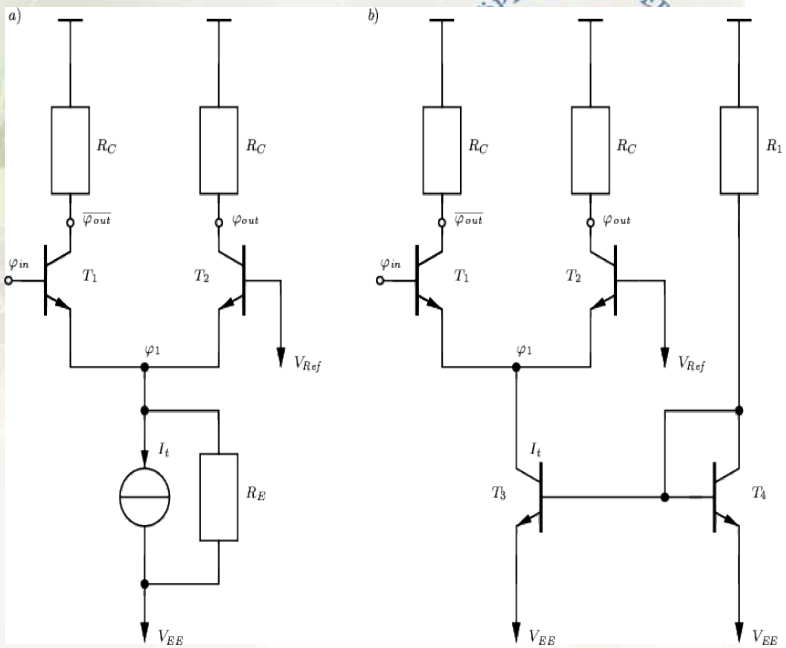
Maximum speed ~ 1 GHz

Limited swing (negative levels and second termination rail).

"Simple/complex"

Power consumption high in quiescent operation
High input impedance and low output impedance

CML (Current-mode logic)



Differential, bipolar, CMOS

Current-driven, AC coupled

Maximum speed (on board) ~ 10 GHz

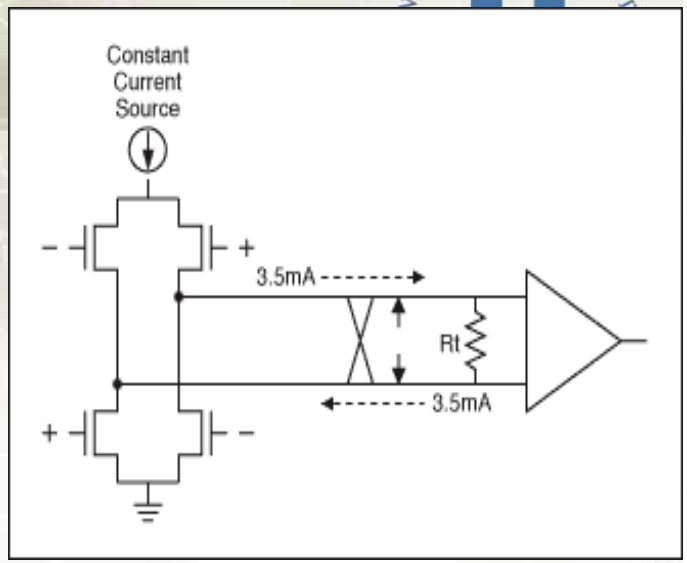
Limited swing: 800 mV terminated to VDD.

Complex.

Power consumption is increasing with frequency and has a high impact on the chip IO ring (large switches and high dI/dt)

Infinite input impedance and low output impedance

LVDS (Low-voltage differential signalling)



Differential, CMOS

Current-driven. Max current of 3.5 mA.

Maximum speed (on board) 2.5 GHz

Limited swing: 350 mV around a center point ~1.25 V

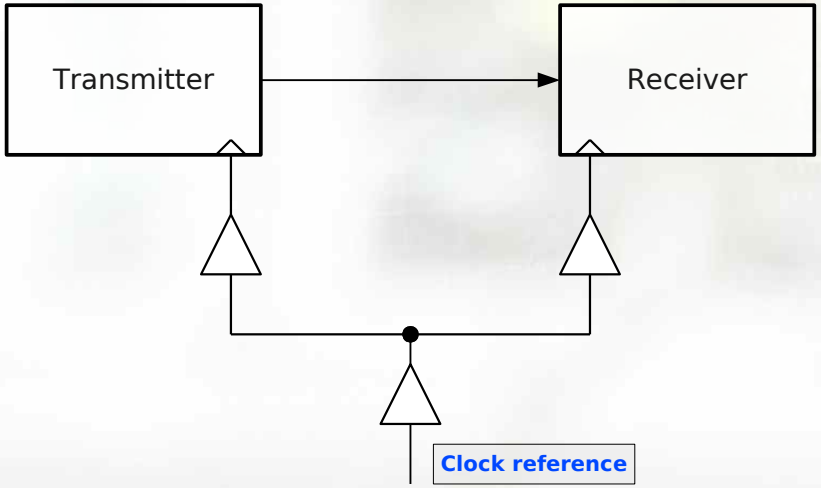
Complex
Comparatively low power for the speed.

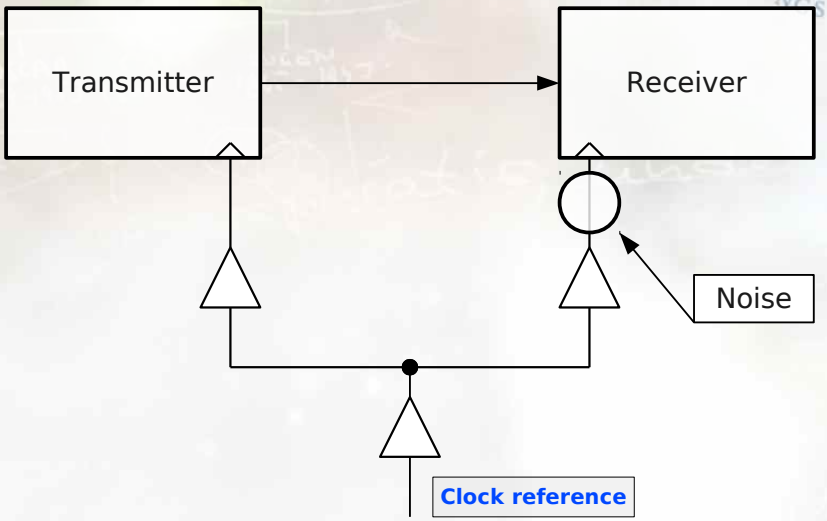
100-Ohm termination (100x3.5 mA ~ 350 mV)

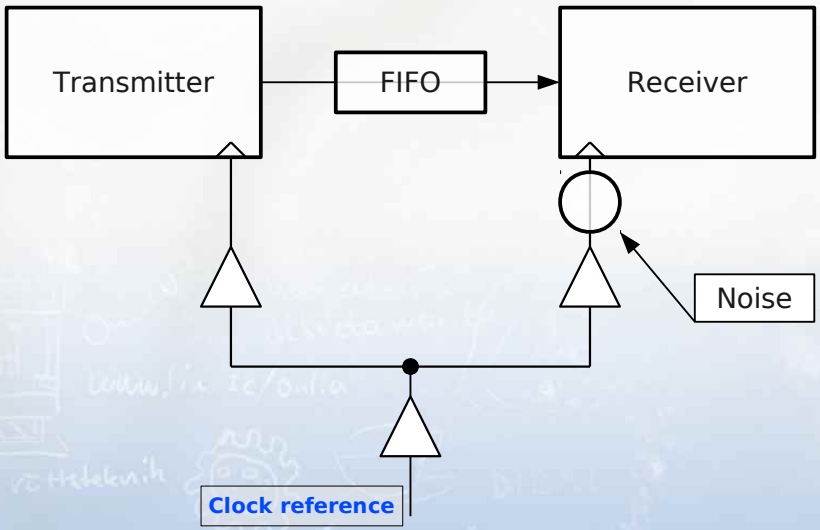
Sammanfattande tabell (exemplifierande siffror)

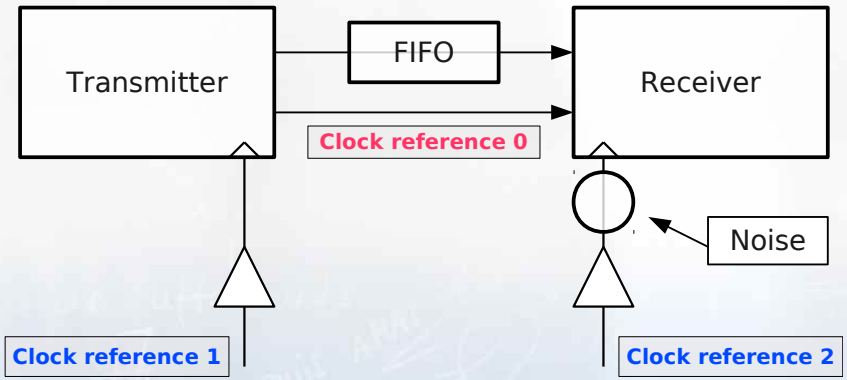
Typ	Hastighet [GHz]	Effekt	Arkitektur	Sving	Anpassning
CMOS	0.5	Ökar med frekvens	Single-ended	Fullt	
LVDS	2.5	Konstant	Differentiell	350 mVpp	Inbyggt
TTL	0.2	Hög, men konstant	Single-ended	Begränsat	
ECL	1	Hög	Single-ended	Begränsat	
CML	10	Hög, men konstant	Differentiell	Begränsat	AC-kopplad (kräver terminering)

Klockning och timing









Clock distribution, brute-force

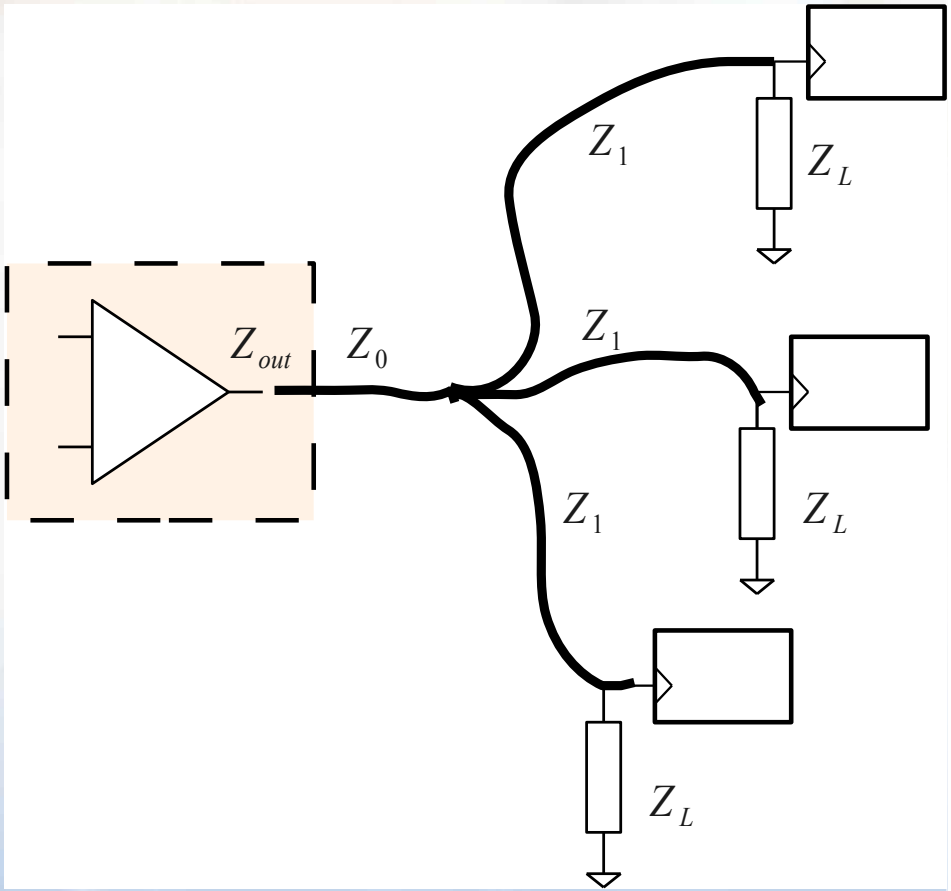
Assuming low-impedance driver $(Z_{out} \approx 0)$

Locate recipients close to each-other

Wave absorbed by the termination at receiver

Drivers cannot drive too many loads - Power consumption!

Put many drivers in parallel



Clock distribution, clock tree

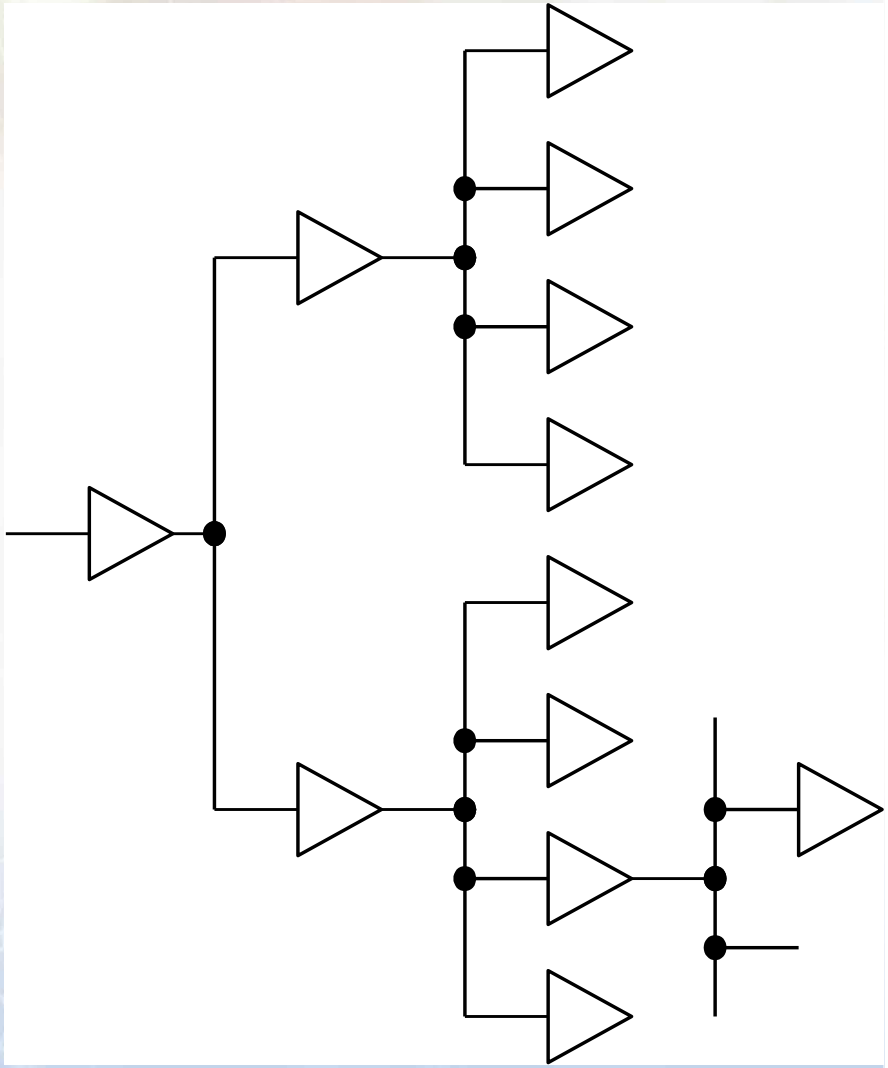
Assuming low-impedance driver

$(Z_{out} \approx 0)$

Minimizes skew (if properly matched)

Intermediate points can be "brute-force"

Tapering factor is lower and less strict requirements on drivers



Clock distribution, lines

Assuming low-impedance driver $(Z_{out} \approx 0)$

Reflected wave at each chip: $-C_g Z_0/2$ and

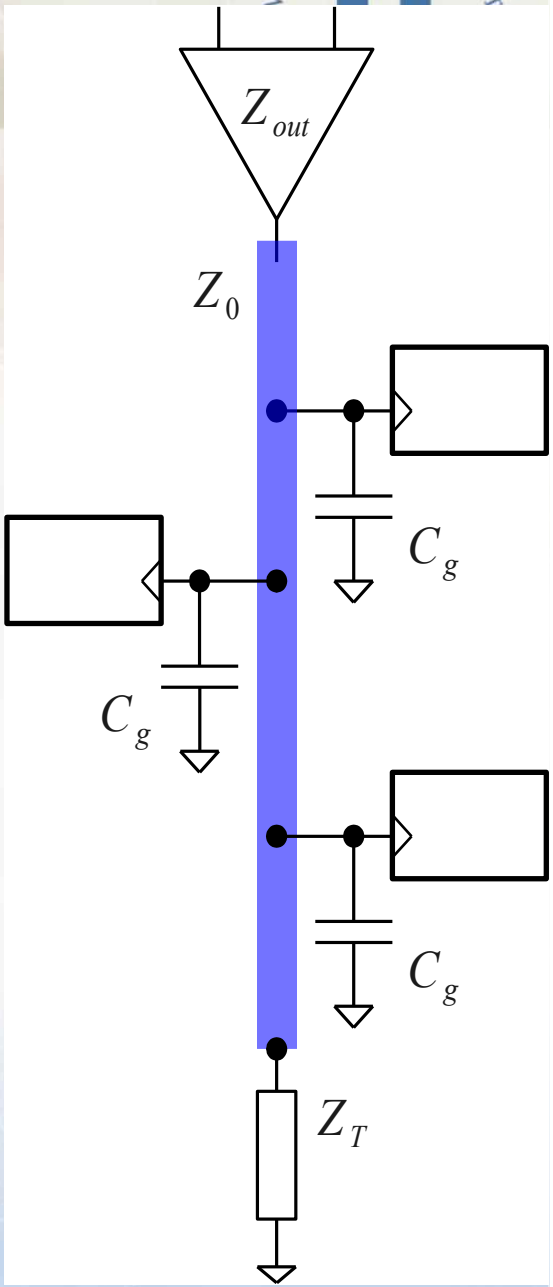
given by the slope of the pulse, $i \sim C_g \cdot dV/dt$

This implies

Reduce the rise/fall times

Minimize the capacitance at each node

Reduce the impedance levels Z_0, Z_T.



Clock distribution, source termination

Assuming "high"-impedance driver, $(Z_{out} > 0)$

Driving N loads **without** far-end (resistive) termination.

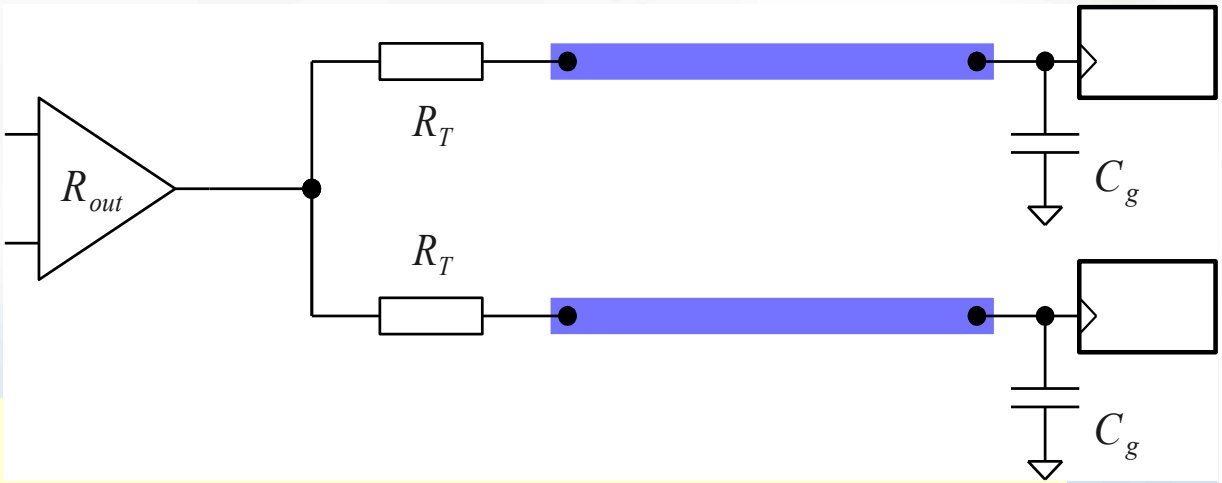
Important (c.f. the lab)

Equal delay required

Equal load required

Choose $R_T = Z_0 - R_{out} \cdot N$

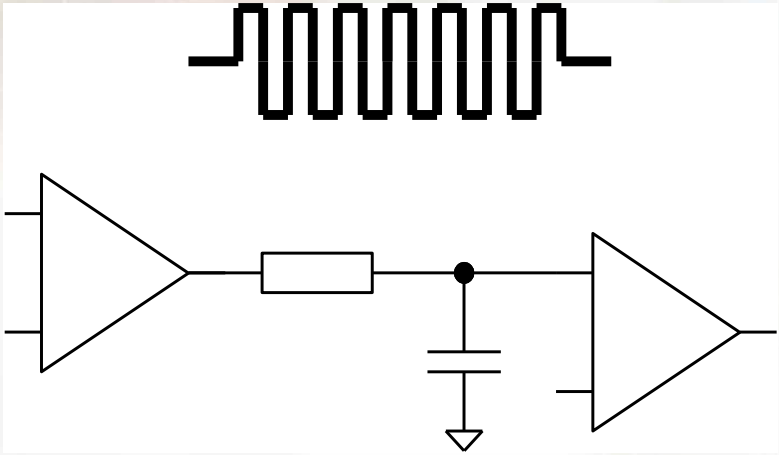
Max R_{out} cannot be too large!



Delay adjustments

Why?

Due to skew and matching (!) we need to guarantee equal length and equal delay



Examples of solutions

Increase length of wires

Introduce extra RC delay

Active tuning of delay

PLL/DLL

Oscillators

Voltage controlled oscillators (VCO)

Frequency controlled by an externally applied voltage.
Continuous-operation over a certain range.

Fixed-frequency oscillators (crystal)

The frequency is tuned to a fixed value (within tolerances).

Digitally controlled oscillators (NCO)

Frequency controlled by an externally applied control word.
Output frequency is given by multiples of a fixed frequency

Oscillators, stability

Different types of sources might influence the frequency

Temperature and voltage dependency

Supply noise and step functions on references

Results in (for example)

Jitter: cycle-to-cycle jitter, phase-noise

Drift in frequency: longer time spans, long-term jitter (LTJ)

A shift in nominal frequency (frequency offset)

Example (due to offset)

Assume a serial sequence of $N = 1024$ bytes.

Transmitter uses a f_0 clock (1 MHz).

Receiver uses $f_0 + \Delta f$ clock. How large can Δf be?

$$T_{tx} - T_{rx} < \frac{1}{2 \cdot f_{tx}} \Rightarrow \frac{N}{f_0} - \frac{N}{f_0 + \Delta f} < \frac{1}{2 f_0} \Rightarrow \Delta f < \frac{f_0}{2N - 1}$$

, i.e., $\Delta f < 0.5$ kHz

Example (clock drift due to jitter)

Assume a serial sequence of $N = 1024$ bytes.

Transmitter uses a f_0 clock (1 MHz), but has a cycle-to-cycle jitter of $\sigma_{CC} = 0.01$ (1 % is a very large value ...).

How large is the deviation at the last bit of the sequence?

A random-walk process. The Long-term jitter is

$\sigma_{LTJ} = \sqrt{N} \cdot \sigma_{CC}$, i.e., $\sigma_{LTJ} \approx \sqrt{1024} \cdot 0.01 \approx 0.3$ (30% = 300kHz!)

Drift due to jitter (cycle-to-cycle and long-term jitter) and unmatched tolerances in reference clocks.

Clock synchronization

Phase locked loop (PLL) for jitter/drift

Delay locked loop (DLL) for offsets

Tuned delay (Higher-level PLL/DLL for a more fixed alignment)

Phase-locked loops (PLL)

Local frequency multiplier

A way to multiply a clock frequency (up and down)

Regulation loop comparing reference frequency with output frequency

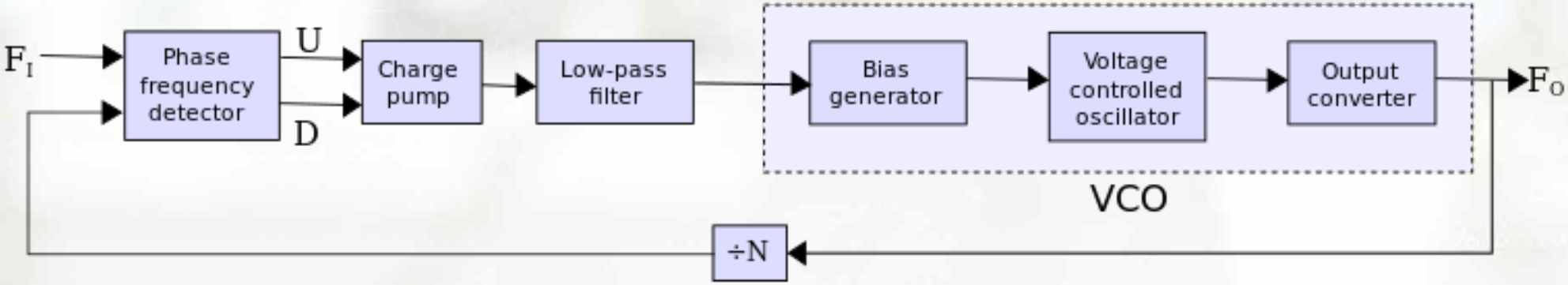
Clock recovery

Synchronize local clock with remote clock

Clock could be embedded in data or transmitted separately

Two slightly different regulation scenarios

PLL, blockschema [Wikipedia]



PLL komponenter

Komponenter

Phase detector

Loop filter

Voltage-controlled oscillator (VCO)

Divider (counter)

Phase comparison! **Phase** locked loop.

Voltage-controlled oscillator

General

$$V_{osc}(t) = V_0 \cdot \sin\left(\omega_0 t + \varphi(t)\right)$$

Phase and frequency relationship

$$\omega(t) = \frac{d\varphi(t)}{dt}, \text{ i.e., } \varphi(s) = \frac{1}{s} \cdot \omega(s)$$

Commonly (desired)

Linear relationship between control and frequency

$$\omega(t) = K_{VCO} \cdot V_{ctrl}(t)$$

Divider (counter)

A "simple" clock divider will be a counter, i.e.,

$$\omega_{div}(t) = \frac{\omega(t)}{N}$$

$$\varphi_{div}(t) = \frac{\varphi(t)}{N}$$

$$\varphi_{div}(s) = \frac{\varphi(s)}{N}$$

Phase detector

Operation

Compares the input phase with the feedback phase

Generate a voltage or current pulse with area/power proportional to phase difference duration

$$I_{pd} = K_{pd} \cdot \varphi_d = K_{pd} \cdot (\varphi_{in} - \varphi_d) = \frac{I_{ch}}{2\pi} \cdot (\varphi_{in} - \varphi_d)$$

Example of phase detector

Waveform diagrams

Loopfilter

Due to the charge peaks we need to slow down and average (integration) the system response by using a loop filter.

At the same time we need to maintain a proportional part in order to react on the phase detector (charge pump)

$$H(s) = K_{lp} \cdot \left(\frac{1}{s} + \frac{1}{p_{lp}} \right)$$ (PI-regulator)

Commonly

$K_{lp} \approx \frac{1}{C_s}$ and $p_{lp} \approx \frac{1}{RC_s}$, $C_p \ll C_s$, i.e., $H(s) \approx \frac{1}{C_s} \cdot \left(\frac{1 + sRC_s}{s} \right)$

PLL model

Storsignalmodell

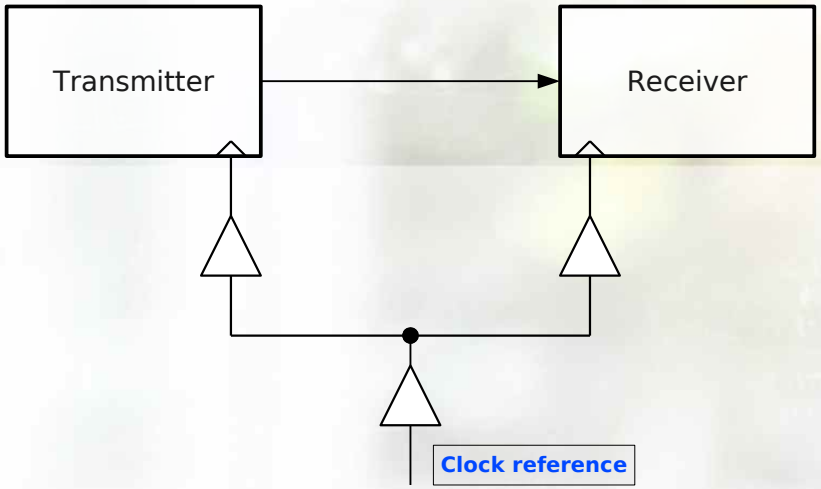
$$H_{PLL}(s) = \frac{1}{p_y^2} \cdot \frac{s^2}{1 + s/p_{lp} + s^2/\omega_y^2}$$, with $$p_y = \sqrt{\frac{K_{pd} \cdot K_{lp} \cdot K_{osc}}{N}}$$

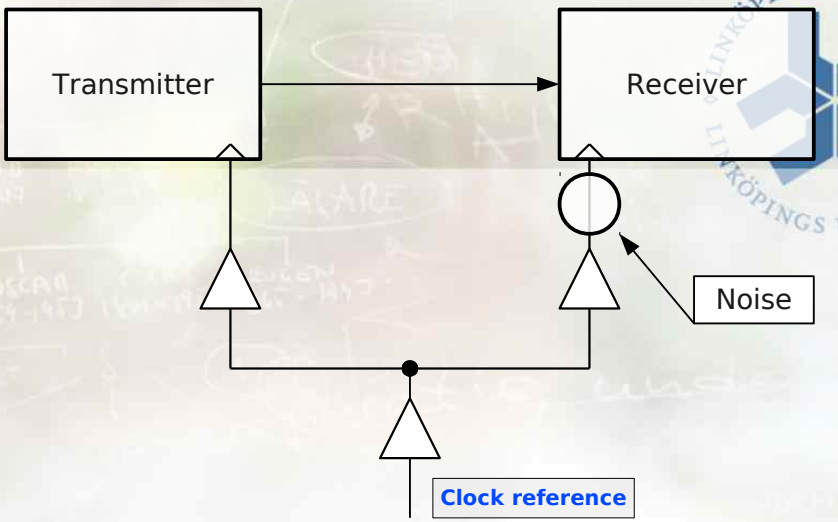
Småsignalmodell (jämför bilden)

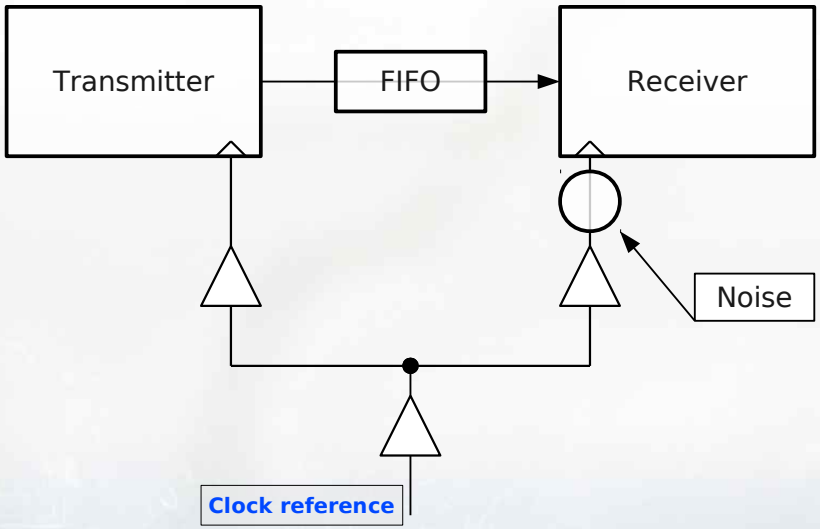
$$H_{PLL}(s) = N \cdot \frac{1 + s/p_{lp}}{1 + s/p_{lp} + s^2/p_y^2}$$

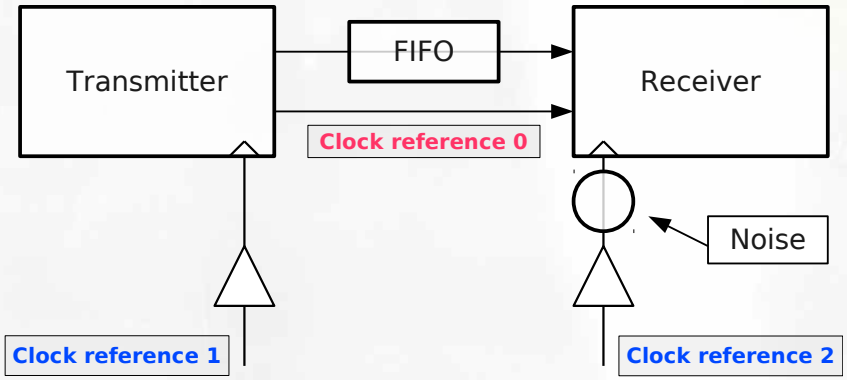
Second-order system with overshoot and peaking, etc.

A trade-off (again): Jitter (noise) vs frequency tracking.


Transmitter
Receiver
Clock reference


Transmitter
Receiver
Noise
Clock reference


Transmitter
FIFO
Receiver
Noise
Clock reference


Transmitter
FIFO
Receiver
Clock reference 0
Noise
Clock reference 1
Clock reference 2

Communication scenarios

Choice of PLL depends on your system and your requirements.

Two examples

Fast varying clock

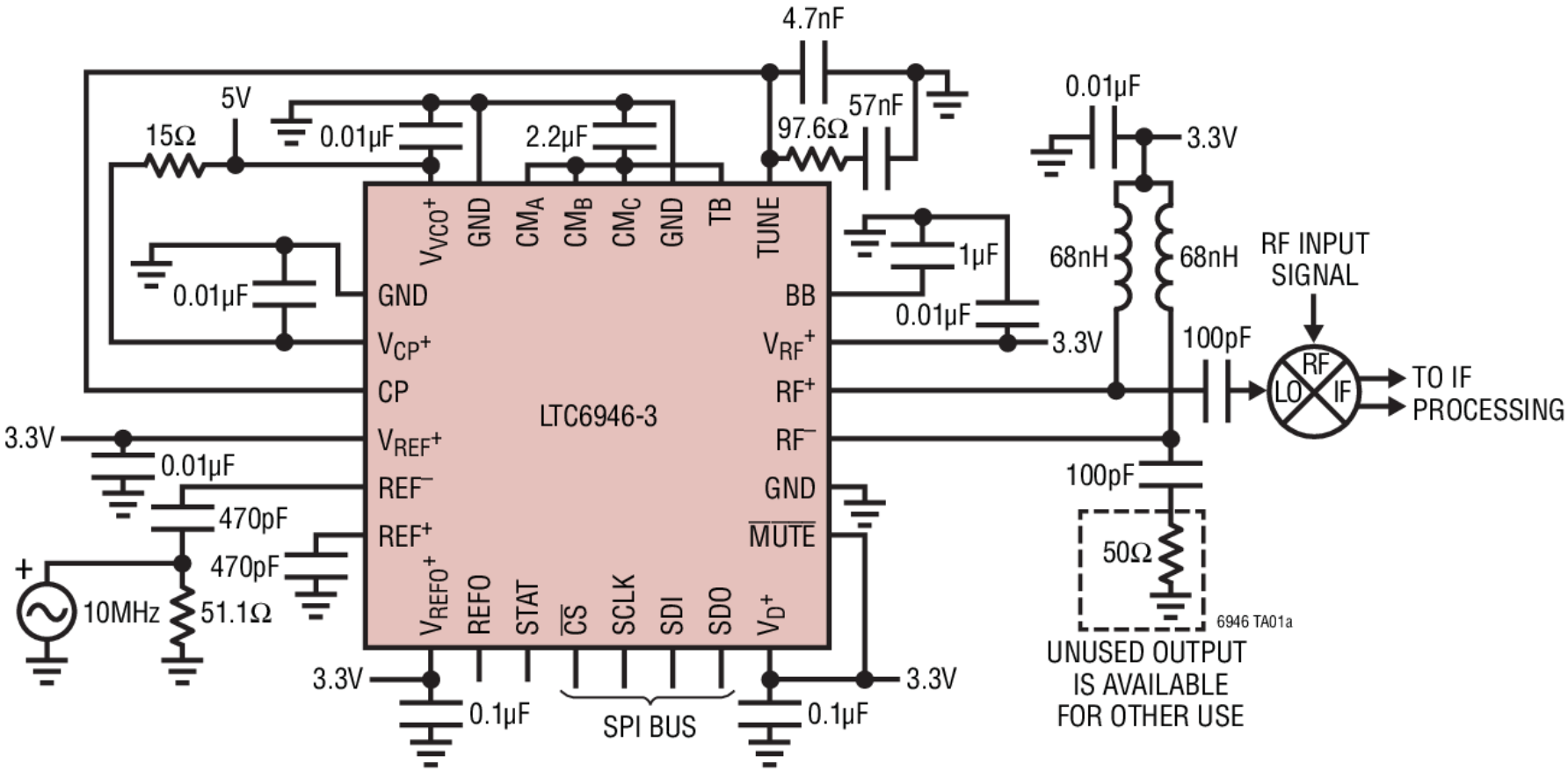
Rx system is dependent on Tx clock

Slow-varying clock:

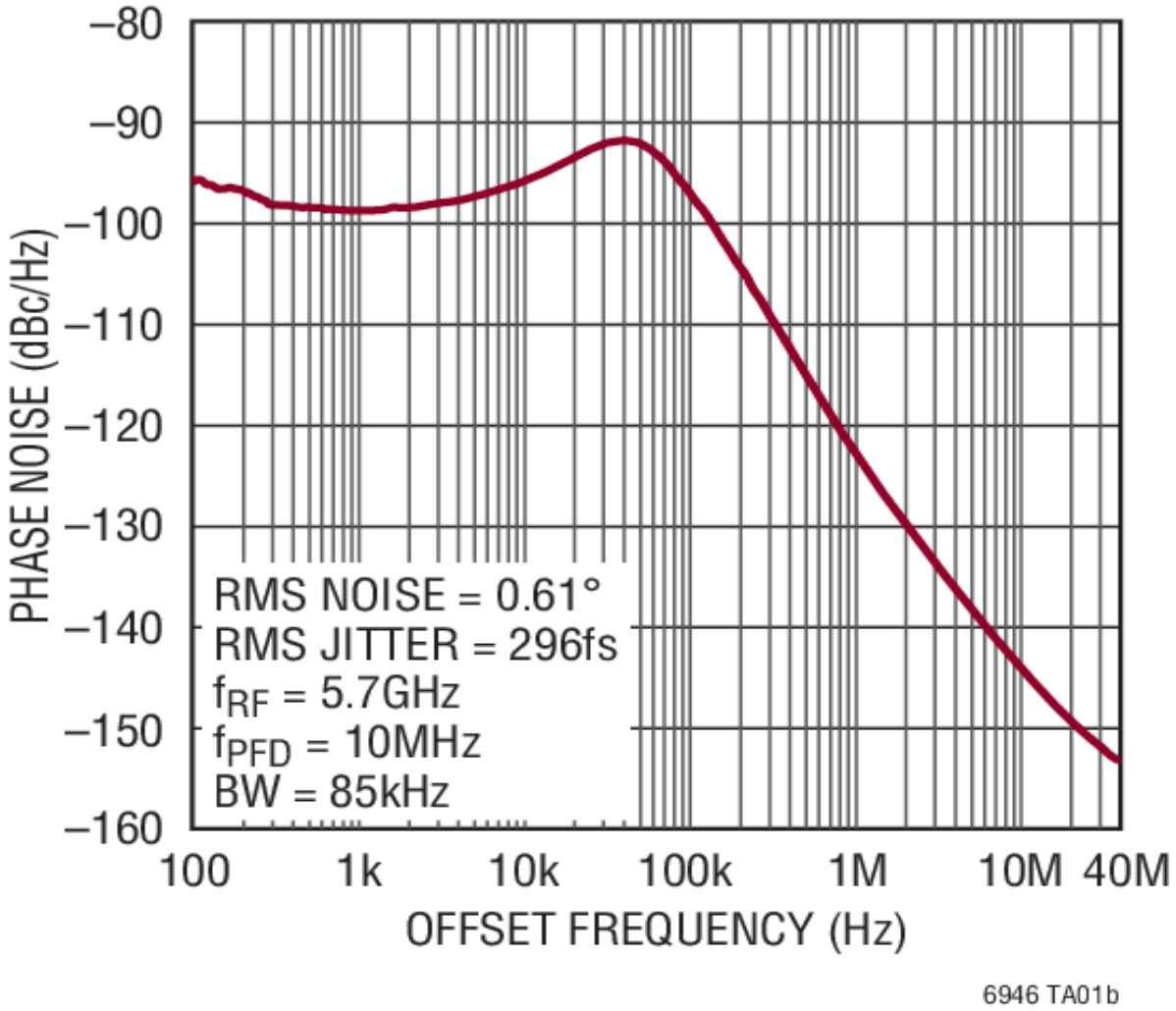
Rx system and Tx system track the same crystal

LTC6946

5.7GHz Wideband Receiver



LTC6946


LTC6946-3 PLL Phase Noise
PHASE NOISE (dBc/Hz)
–80
–90
–100
–110
–120
–130
–140
–150
–160
RMS NOISE = 0.61°
RMS JITTER = 296fs
fRF = 5.7GHz
fPFD = 10MHz
BW = 85kHz
100
1k
10k
100k
1M
10M
40M
OFFSET FREQUENCY (Hz)
6946 TA01b

Vad gjorde vi idag?

Snabb koll på avkopplingskondensatorer

Impedance of the supply net

Signal and clock distribution

Three different ways

Use differential signals!

Balance the paths

Oscillatorer och klockkällor

Vad står på tur nästa gång?

Miscellaneous blocks

PLL and DLL

Regulators

Föreläsning 10, Gott och blandat

Faslåsta loopar
Regulatorer

Vad gjorde vi förra gången?

Timing, clock distribution

Tapered tree structure

Design guide with respect to termination, number of loads, etc.

Signalling

Differential schemes

TTL, ECL, LVDS, CMOS, etc.

Vad kommer vi göra idag?

Some recapture

Timing and signalling

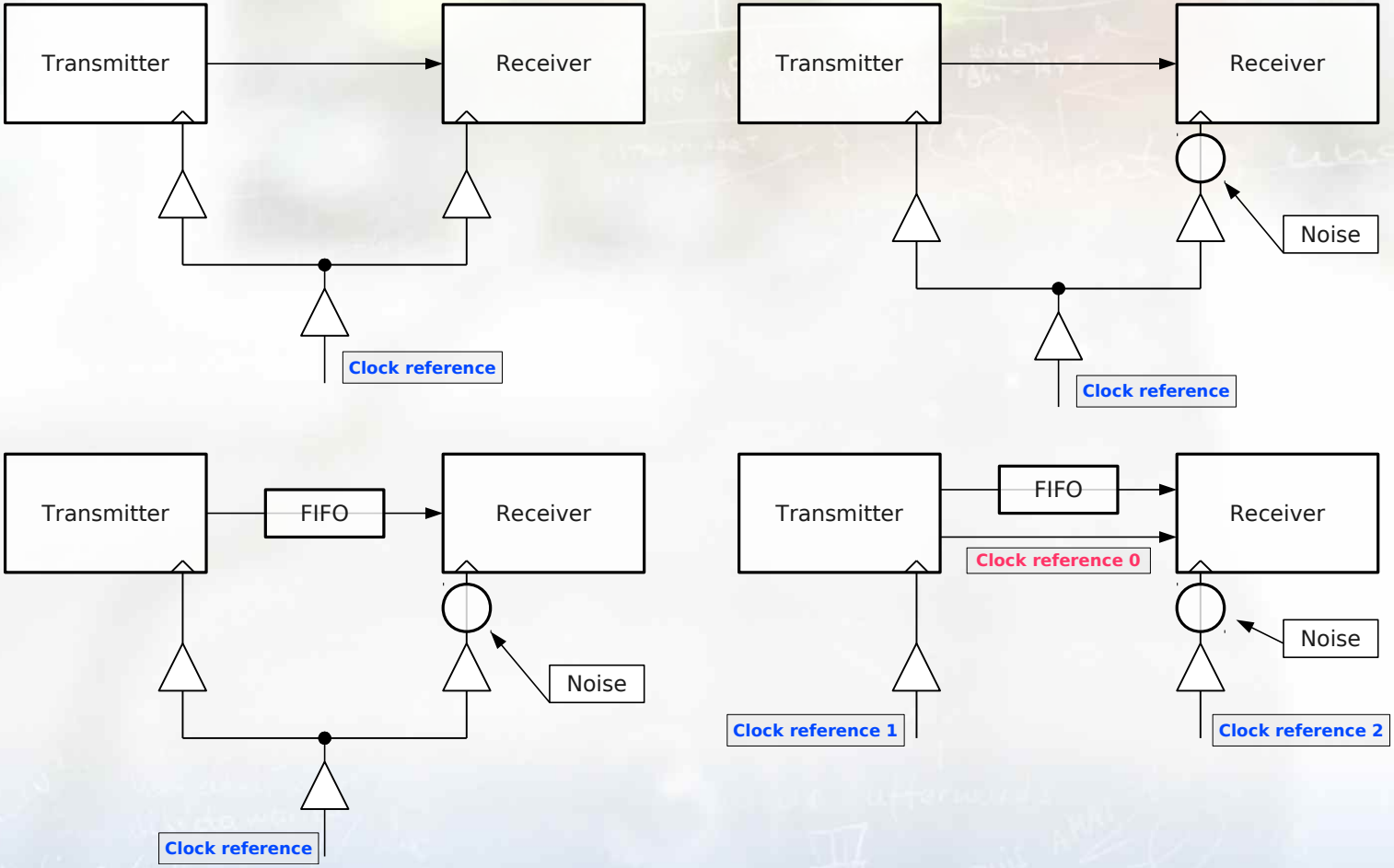
Regulators

Low drop-out regulators (LDO)

Timing

PLL, DLL

Timing revisited



Timing revisited, scenario

Systems communicating could see different clocks

Drift due to jitter (cycle-to-cycle jitter and long-term jitter) and unmatched tolerances in reference clocks.

Example (clock drift)

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PLL blockschema

PLL komponenter

Komponenter

Phase detector

Loop filter

Voltage-controlled oscillator

Divider (counter)

Phase comparison! *Phase* locked loop.

Oscillator

General

$$V_{osc}(t) = V_0 \cdot \sin\left(\omega_0 t + \varphi(t)\right)$$

Phase and frequency relationship

$$\omega(t) = \frac{d\varphi(t)}{dt}, \text{ i.e., } \varphi(s) = \frac{1}{s} \cdot \omega(s)$$

Commonly (desired)

Linear relationship between control and frequency

$$\omega(t) = K_{VCO} \cdot V_{ctrl}(t)$$

Divider (counter)

A "simple" clock divider will be a counter, i.e.,

$$\varphi_{div}(t) = \frac{\varphi(t)}{N}, \text{ i.e., } \varphi_{div}(s) = \frac{\varphi(s)}{N}$$

Phase detector

Operation

Compares the input phase with the feedback phase

Generate a voltage or current pulse with area/power proportional to phase difference duration

$$I_{pd} = K_{pd} \cdot \varphi_d = K_{pd} \cdot (\varphi_{in} - \varphi_d) = \frac{I_{ch}}{2\pi} \cdot (\varphi_{in} - \varphi_d)$$

Example of phase detector

Waveform diagrammes

Loopfilter

Due to the charge peaks we need to slow down and average (integration) the system response by using a loop filter.

At the same time we need to maintain a proportional part in order to react on the phase detector (charge pump)

$$H(s) = K_{lp} \cdot \left(\frac{1}{s} + \frac{1}{\omega_{lp}} \right)$$

Commonly

$K_{lp} \approx \frac{1}{C_s}$ and $\omega_{lp} \approx \frac{1}{R C_s}$, $C_p \ll C_s$, i.e., $H(s) \approx \frac{1}{C_s} \cdot \left(\frac{1 + s R C_s}{s} \right)$

PLL model

Large signal model

$$H_{PLL}(s) = \frac{1}{\omega_y^2} \cdot \frac{s^2}{1 + s/\omega_{lp} + s^2/\omega_y^2}$$, with $$\omega_y = \sqrt{\frac{K_{pd} \cdot K_{lp} \cdot K_{osc}}{N}}$$

Small-signal model

$$H_{PLL}(s) = N \cdot \frac{1 + s/\omega_{lp}}{1 + s/\omega_{lp} + s^2/\omega_y^2}$$

Second-order system with overshoot and peaking, etc.

A trade-off (again): Jitter vs frequency tracking.

Communication scenarios

Choice of PLL depends on your system and your requirements.

Two examples

Fast varying clock

Rx system is dependent on Tx clock

Slow-varying clock:

Rx system and Tx system track the same crystal

Delay-locked loop

Even though PLL is phase-driven, it locks the frequency.

At some points, you want to change the phase given a certain clock frequency.

Scenario

You have a stable frequency to data clock.

Data arrives however on say three different ports, but with different delays.

With a delay-locked loop you can adjust the phase without touching the frequency.

Delay-locked loop

Similar to PLL

Example diagram

Voltage regulators

A modern hand-held system could have up to 20+ regulators.

Why different supplies?

Minimize power consumption in digital circuitry

Power amplifiers, RF circuits, display drivers, bus drivers

Different standards imply different voltage levels

Isolation between supplies

Compensate for drift in batteries, etc.

Voltage regulators, specifics

A regulator should ...

Take an input voltage and produces an output voltage

be power efficient, i.e., no losses

different load conditions (no current, max current, spiking)

handle drift in the input voltage (loss in battery voltage, etc.)

Add-ons

Output could be both higher and lower than input voltage

Power down modes (supply switching)

Low-drop out regulators (LDO)

First try

Just a resistor. Current through the resistance forms the drop.
Will be current dependent!

Second try

Use voltage divider on input and compare with output voltage.
Drive pass-transistor PMOS (actually it could be in saturation)

Third try

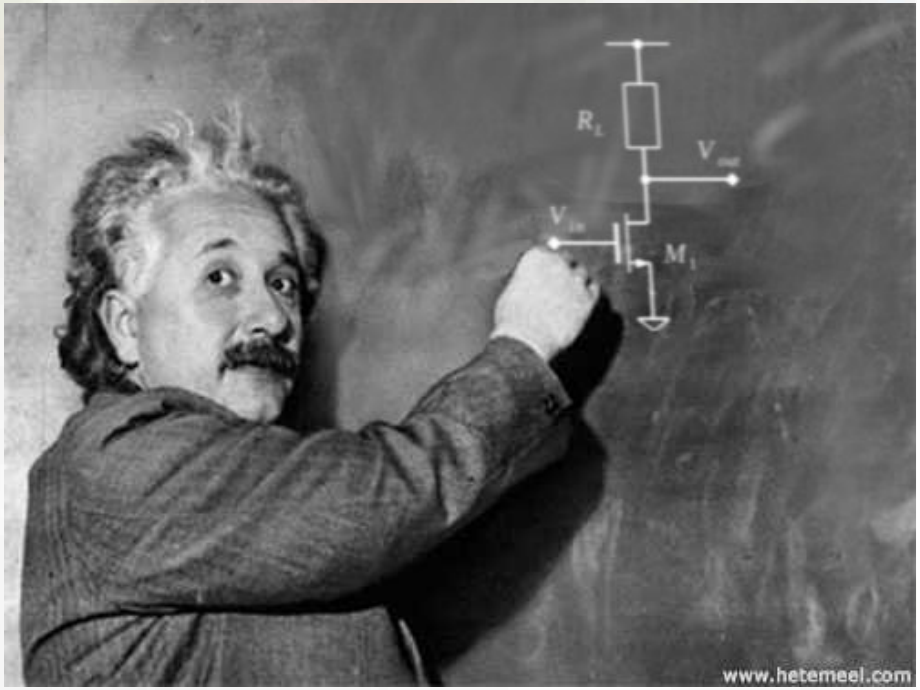
Use voltage divider on output and compare with reference.
Drive pass-transistor gate (actually it could be in saturation)

Low-drop out regulators, cont'd

Output impedance

At DC, $Z_{out} \approx 0$.

At HF, $Z_{out} \approx Z_{load}$



Three poles

Dominant pole (error amplifier)

Second pole (output load) !!!

Third pole (parasitic elements)

Low-drop out regulators, cont'd

Load regulation

Changes in the impedance of the load

Current spikes (switched devices) influences the load impedance

Line regulation

Changes in the input (or reference) voltage

Cost measure

$$\eta = \frac{V_{max} - V_{min}}{V_{nom}}$$

Regulators, misc

Voltage boosting

The drop-out might not be large enough

Increase the gate voltage

Switched-mode regulators

Out of the scope of this course, see Kent's course

Vad står på tur nästa gång?

Tenta!

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