EXERCISE SECTION 15: TIMING AND MISCELLANEOUS

15.1. Loop filter of a PLL

Find the loop filter gain constant K_{lp} and ω_z for the circuit with a C_2 in parallel with R_1 and C_1 which are in series. $R_1 = 10\ k$, $C_1 = 0.1\,\mu F$, $C_2 = 0.01\,\mu F$.

15.2. Sources of Jitter and skew

a. A balanced clock distribution scheme is shown in Figure 0.2. For each source of variation, identify if it contributes to skew or jitter. Circle your answer in Table 0.1

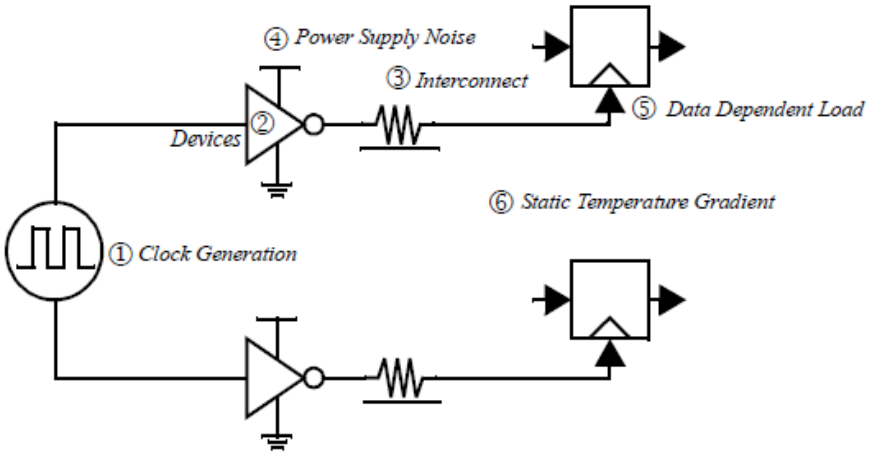

Figure 0.2 Sources of Skew and Jitter in Clock Distribution.

1) Uncertainty in the clock generation circuit	Skew	Jitter
2) Process variation in devices	Skew	Jitter
3) Interconnect variation	Skew	Jitter
4) Power Supply Noise	Skew	Jitter
5) Data Dependent Load Capacitance	Skew	Jitter
6) Static Temperature Gradient	Skew	Jitter

Table 0.1 Sources os Skew and Jitter