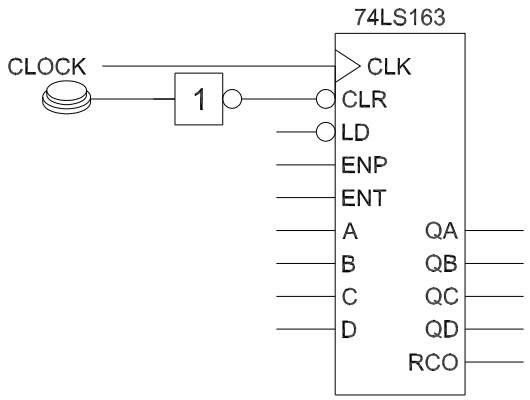
DUGGA 3, TMEL 53, 2017/02/24

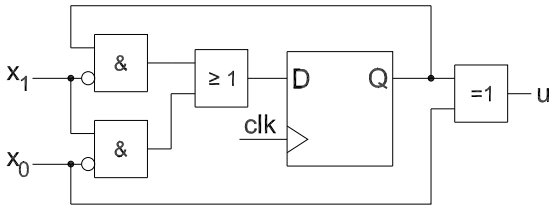
To pass the dugga you have to obtain 7 points out of 10.

EXERCISE 1: The counter in the figure is a 4-bit binary counter (räknare) with synchronous CLR. When the button is pressed the counter is cleared. Then, when the button is released, the counter starts to count. Do the necessary connections (using logic gates) so that the counter counts according to $\underbrace{0}_{CLR}$,1,2,3,4,11,12,13,14 and **stops at 14.** (2p.)

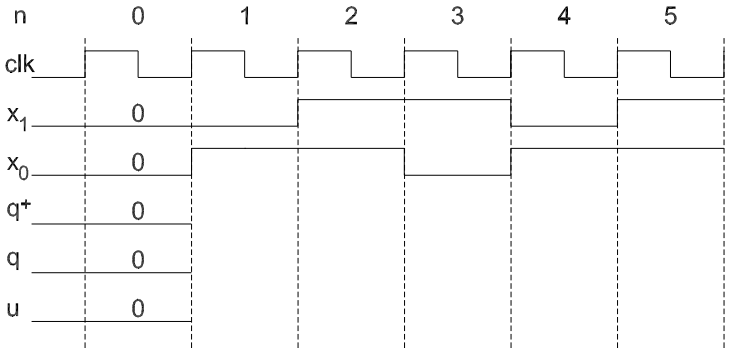
Hint: Double check for which numbers of the count (there might be more than one) the signals LD, ENP and ENT are active.



EXERCISE 2: Reply to the following questions for the circuit in the figure:



a) Is a state machine of type Mealy or Moore? Why? (1p.)
b) Draw the state diagram (tillståndsdiagram). (2p.)
c) Complete the timing diagram (tidsdiagram) below. (1p.)



EXERCISE 3: Using standard logic gates (grindar) and D-flip flops (D-vippor),

a) Design a 2-bit binary counter (räknare) that counts up when an input signal $x = 1$ and counts down when $x = 0$. Note that the counter goes to 0 when counting up from its maximum value and it goes to its maximum value when counting down from 0. (3p.)

b) If your solution uses four or less logic gates (you may need to use XOR gates). (1p.)